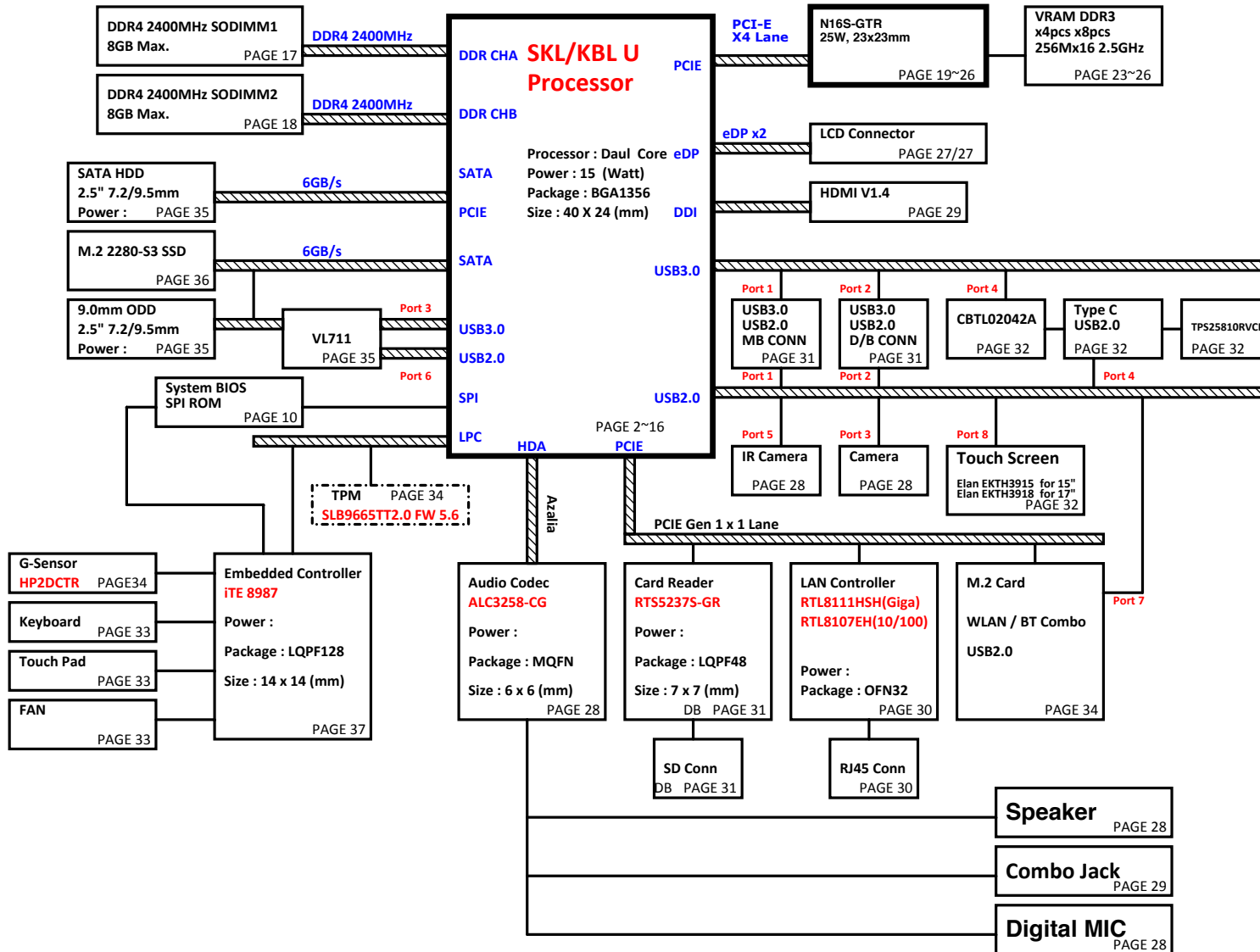


# NFL 2SPD DIS/UMA (15/17")

## Intel SKL/KBL ULT Platform Block Diagram

## PCB 8L STACK UP

LAYER 1 : TOP  
 LAYER 2 : SGND  
 LAYER 3 : IN1(High)  
 LAYER 4 : IN2(Low)  
 LAYER 5 : SVCC  
 LAYER 6 : IN3(High)  
 LAYER 7 : SGND1  
 LAYER 8 : BOT

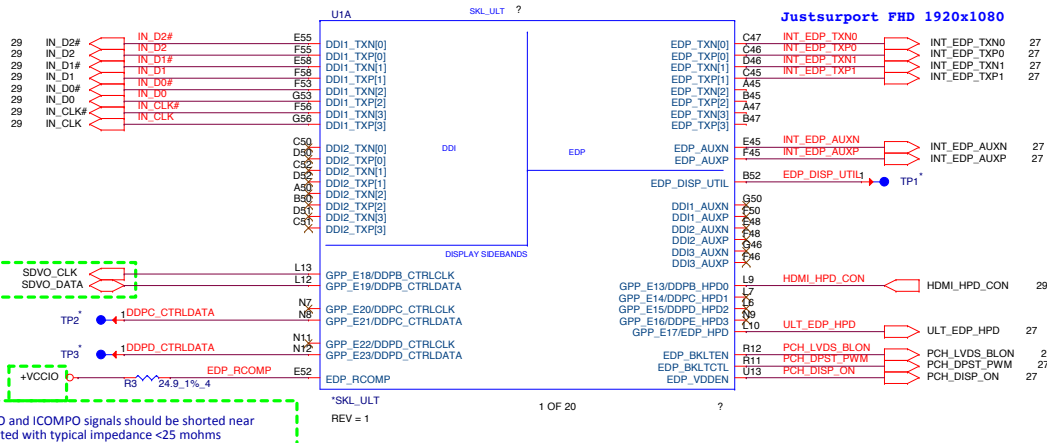


PROJECT : G74A  
 Quanta Computer Inc.

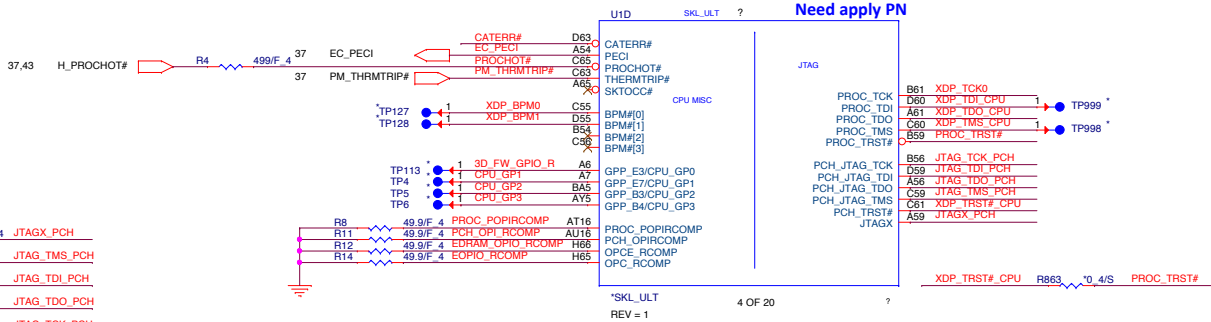
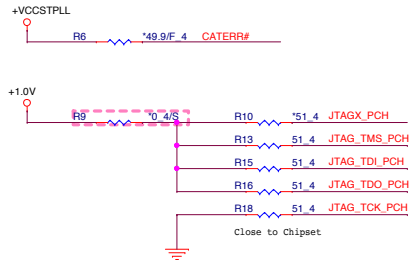
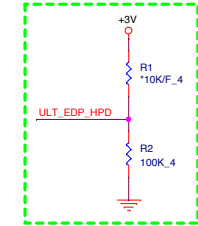
Size Custom Document Number Block Diagram Rev 1A  
 Date: Wednesday, January 11, 2017 | Sheet 1 of 51

+3V 4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51  
+1.0V 4,6,37,42  
+VCCSTPLL 4,5,6,9,42,43

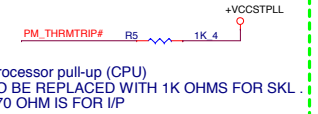
## HDMI



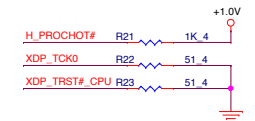
Reserve EDP\_HPD opposites circuit!



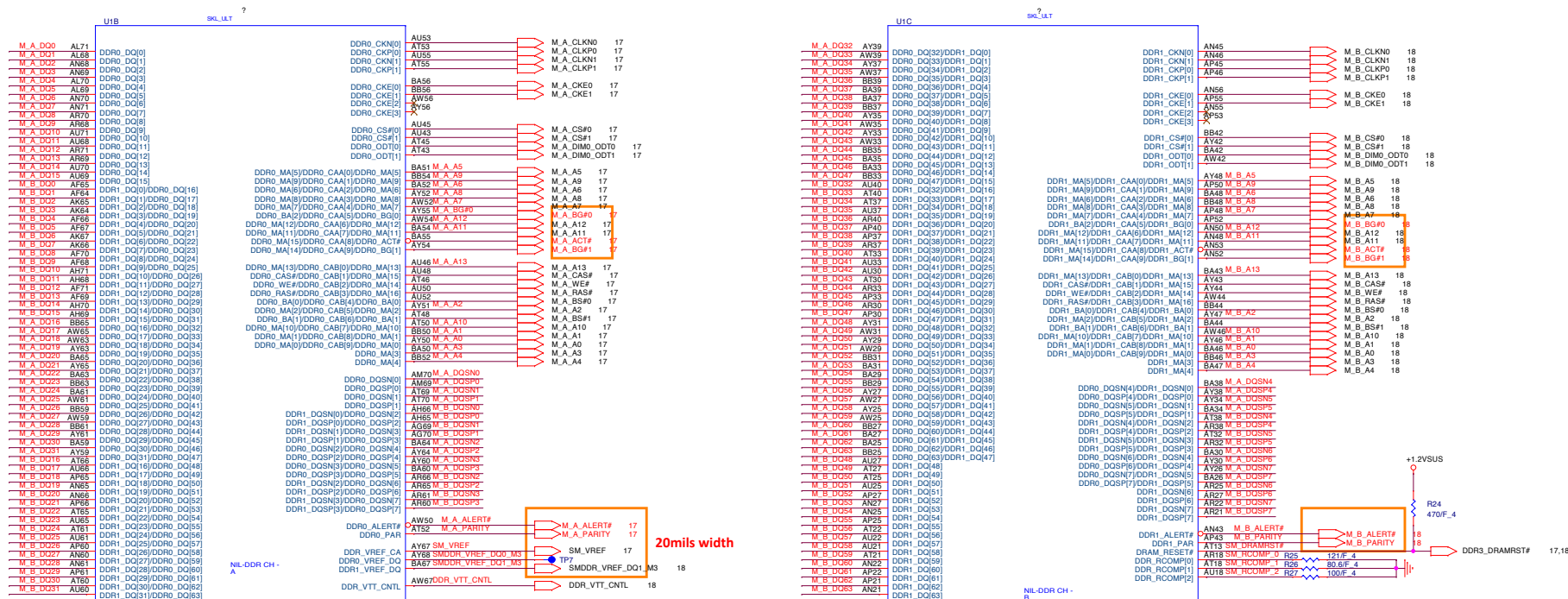
## Close to EC



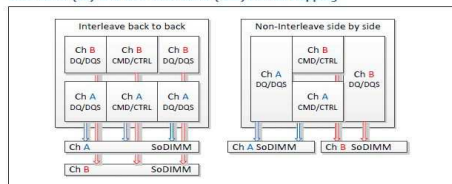
## PLACE NEAR CPU

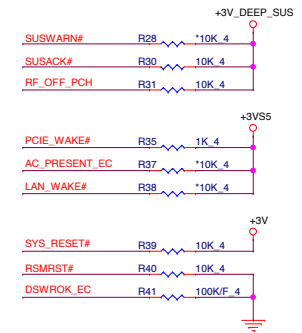


+1.2VSUS 6.17.18.40.42.48



### Interleave (IL) and Non-Interleave (NIL) Modes Mapping

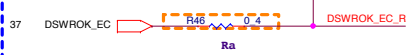




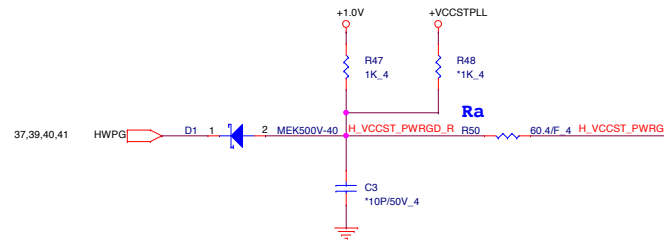
For DS3 -->Ra  
Non-DS3 -->Rb

Rb

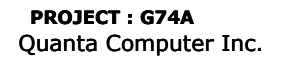
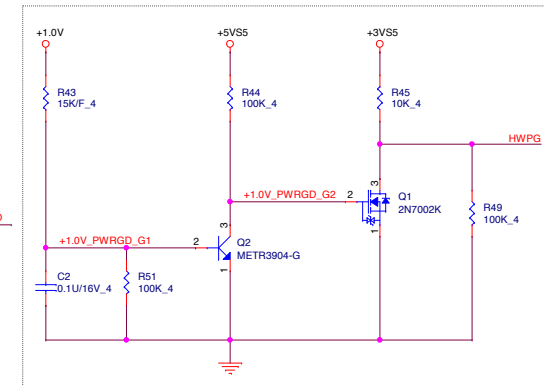
RSMRST# R42 \*0.4



Check Rise/Fall time less than 100ns



**Ra close to CPU side**  
**H\_VCCST\_PWRGD trace 0.3" - 1.5"**

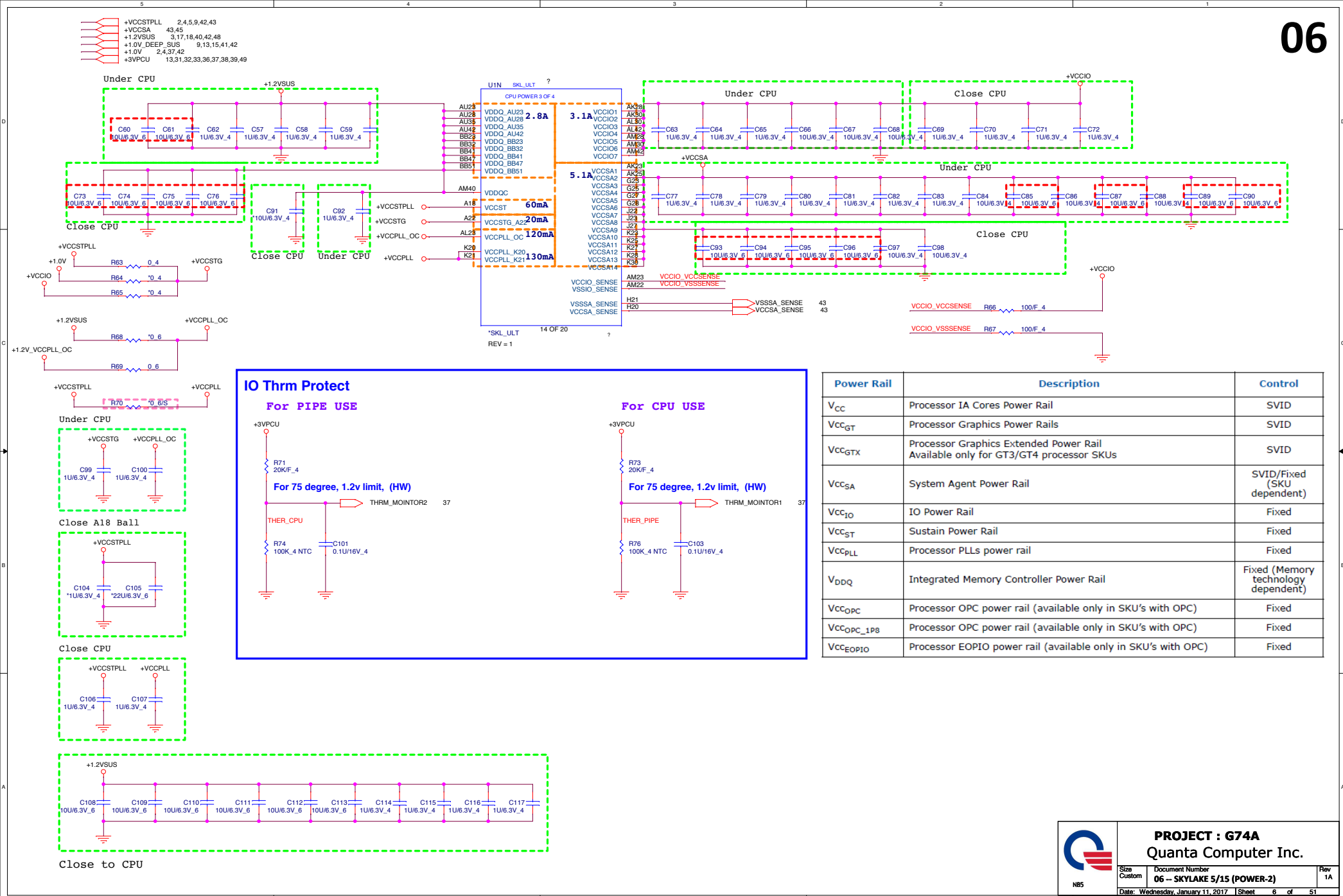


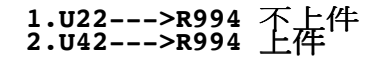
Size Custom	Document Number <b>04 -- SKYLAKE 3/15(PowerManger)</b>	Rev 1A
Date: Wednesday, January 11, 2017	Sheet 4 of 51	




**Layout note: need routing together and ALERT need between CLK and DATA.**

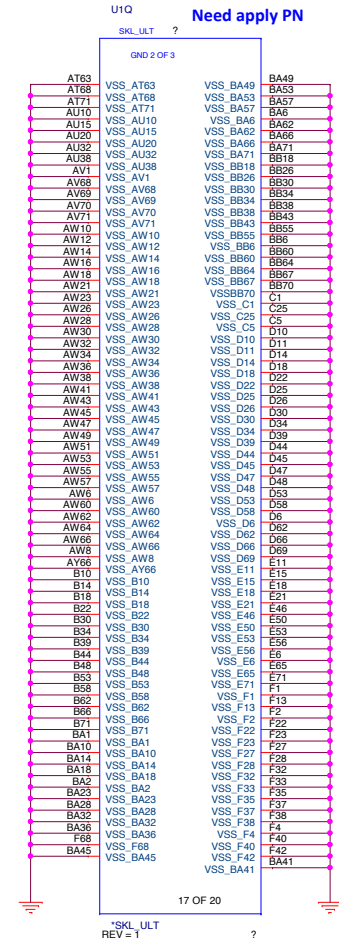
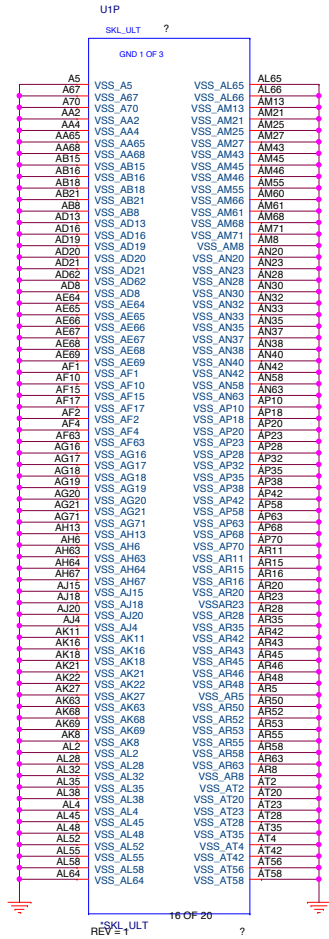
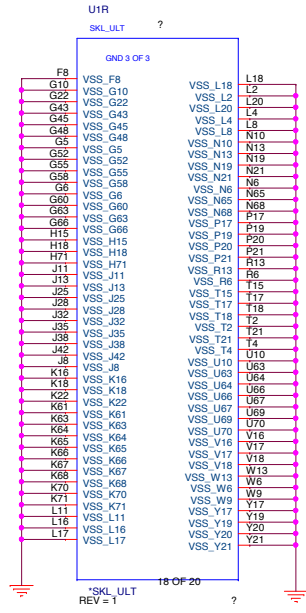







1.U22---C300/C301/C302/C303/C304 不上件  
2.U42---C300/C301/C302/C303/C304 上件

 NB5	<b>PROJECT : G74A</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>07 -- SKYLAKE 6/15 (POWER-3)</b>	Rev 1A
Date: Wednesday, January 11, 2017		Sheet 7 of 51	





**PROJECT : G74A**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>08 -- SKYLAKE 7/15 (GND)</b>	Rev 1A
Date: Wednesday, January 11, 2017   Sheet 8 of 51		







```

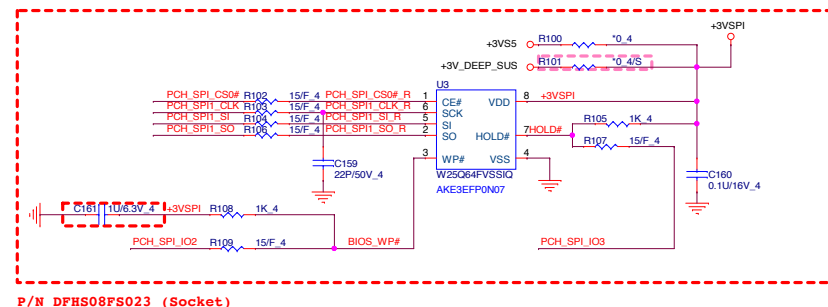
37 PCH_SPI_CS0#_R
37 PCH_SPI1_CLK_R
37 PCH_SPI1_SI_R
37 PCH_SPI1_SO_R

```

TP17	1	PCH_SPI_CS0#_R
TP18	1	PCH_SPI1_CLK_R
TP19	1	PCH_SPI1_SI_R
TP20	1	PCH_SPI1_SO_R
TP21	1	BIOS_WP#
TP22	1	HOLD#

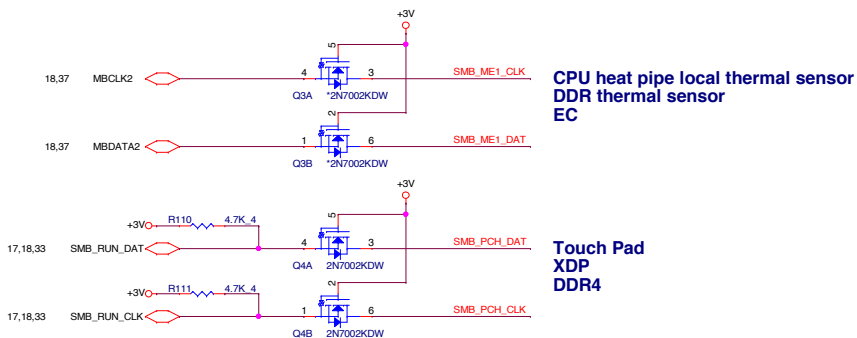
TP size TP2675

## PCH SPI ROM(CLG)



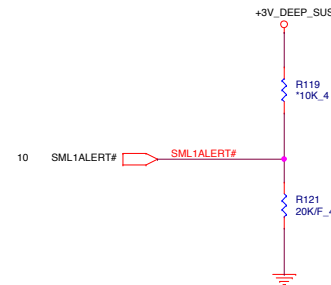
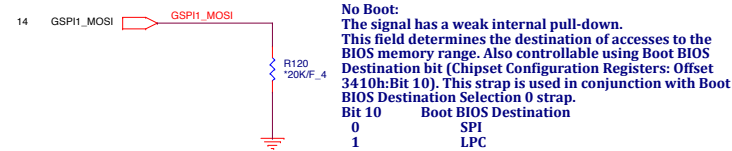
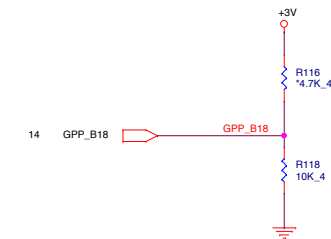
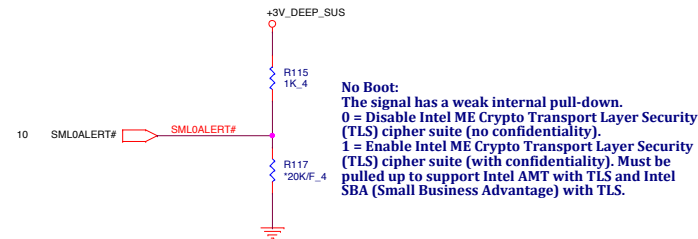
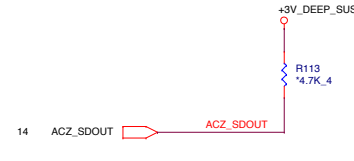
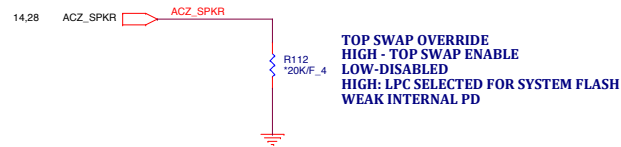
**P/N DFHS08FS023 (Socket)**

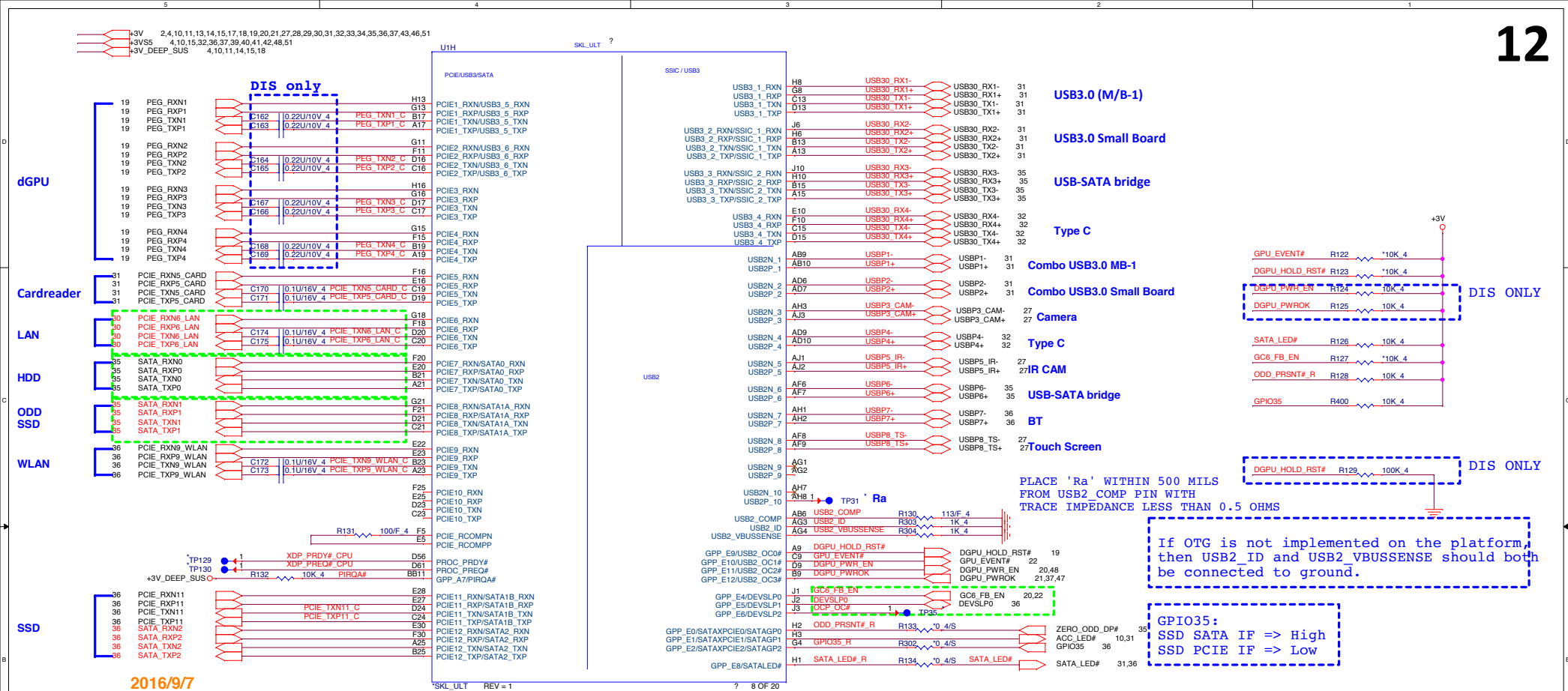
## SMBus/Pull-up(CLG)



# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET





2016/9/7  
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table


PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	CR
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	CardReader	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SSD		
Port9	WLAN		
Port10	Un-used		
Port11	SSDx2		
Port12	SSDx2/ SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 Small Board
PORT-3	USB-SATA bridge
PORT-4	Type C

USB2.0 Port Mapping Table

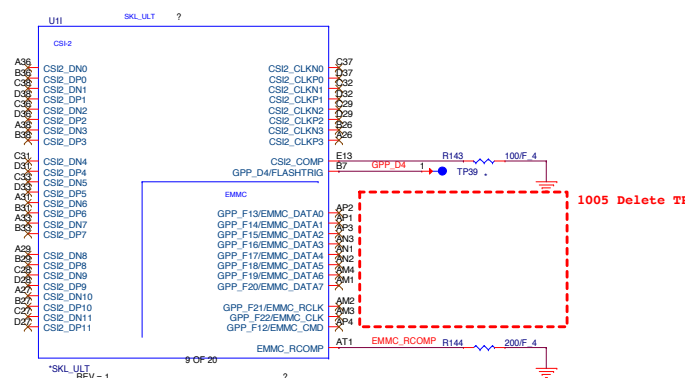
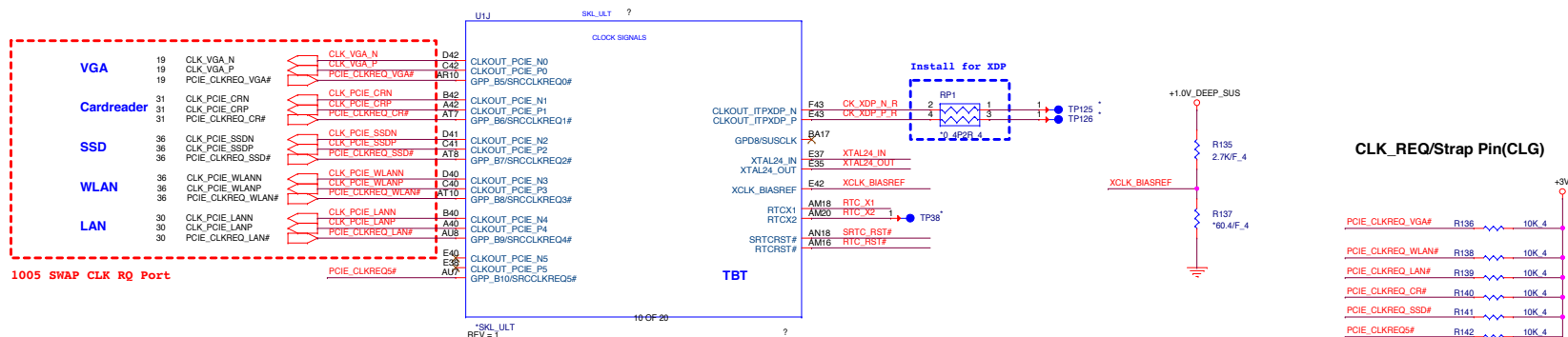
USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	USB-SATA bridge
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC



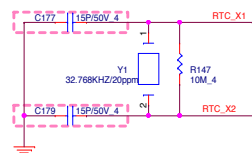
**PROJECT : G74A**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>11 -- SKYLAKE 10/15(HDA)</b>	Rev 1A
Date: Wednesday, January 11, 2017		Sheet 12 of 51

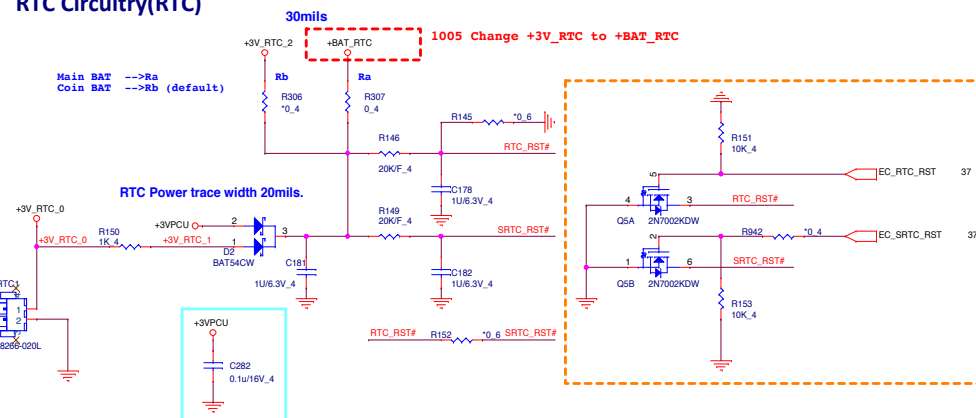
-3V\_RTC\_2 4,15  
 -BAT\_RTC 4,15,33,38,49  
 -1.6V\_DEEP\_SUS 9,15,41  
 -3V 2,4,10,11,12,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51



## RTC Clock 32.768KHz

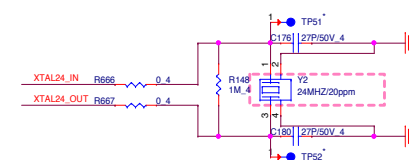


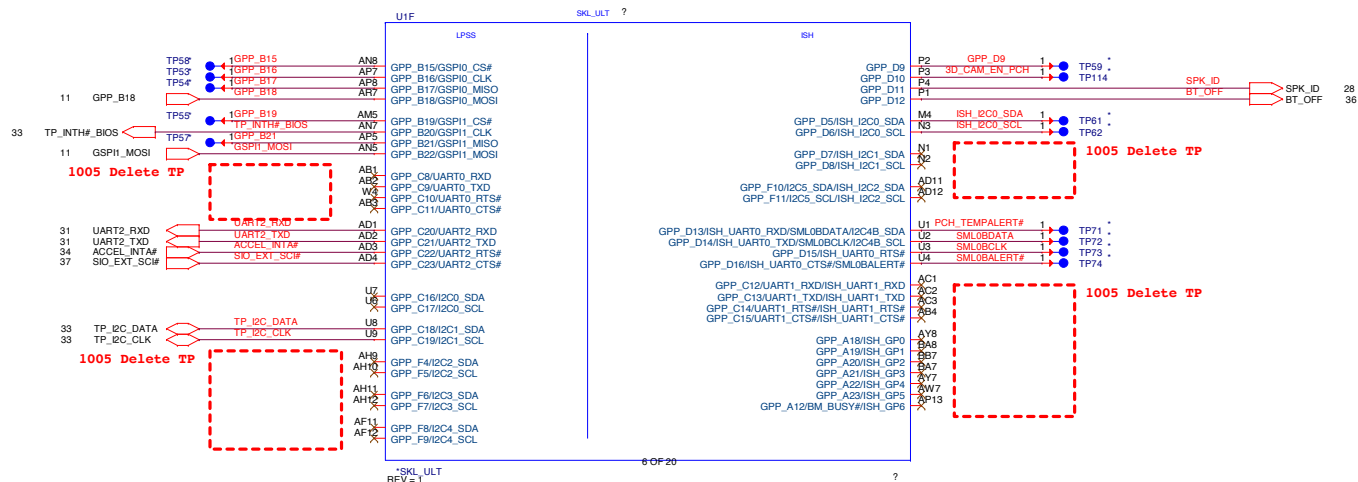
## RTC Circuitry(RTC)



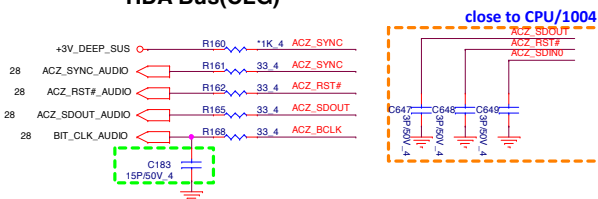
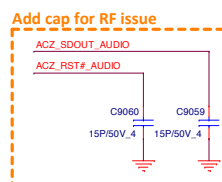
## External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

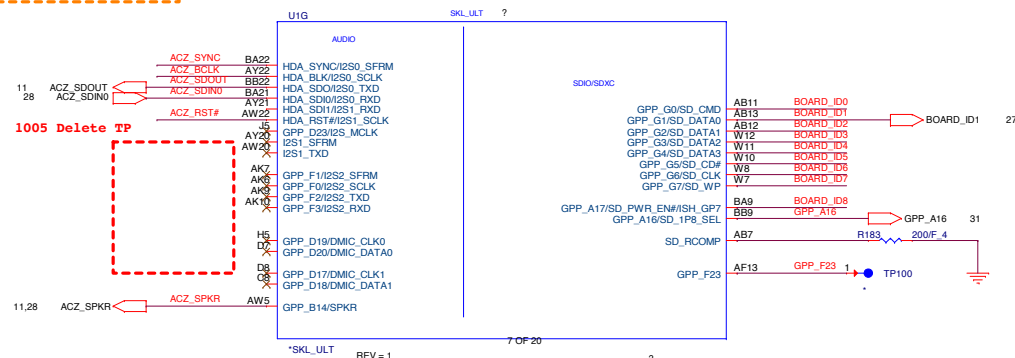


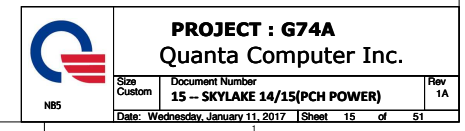


## HDA Bus(CLG)



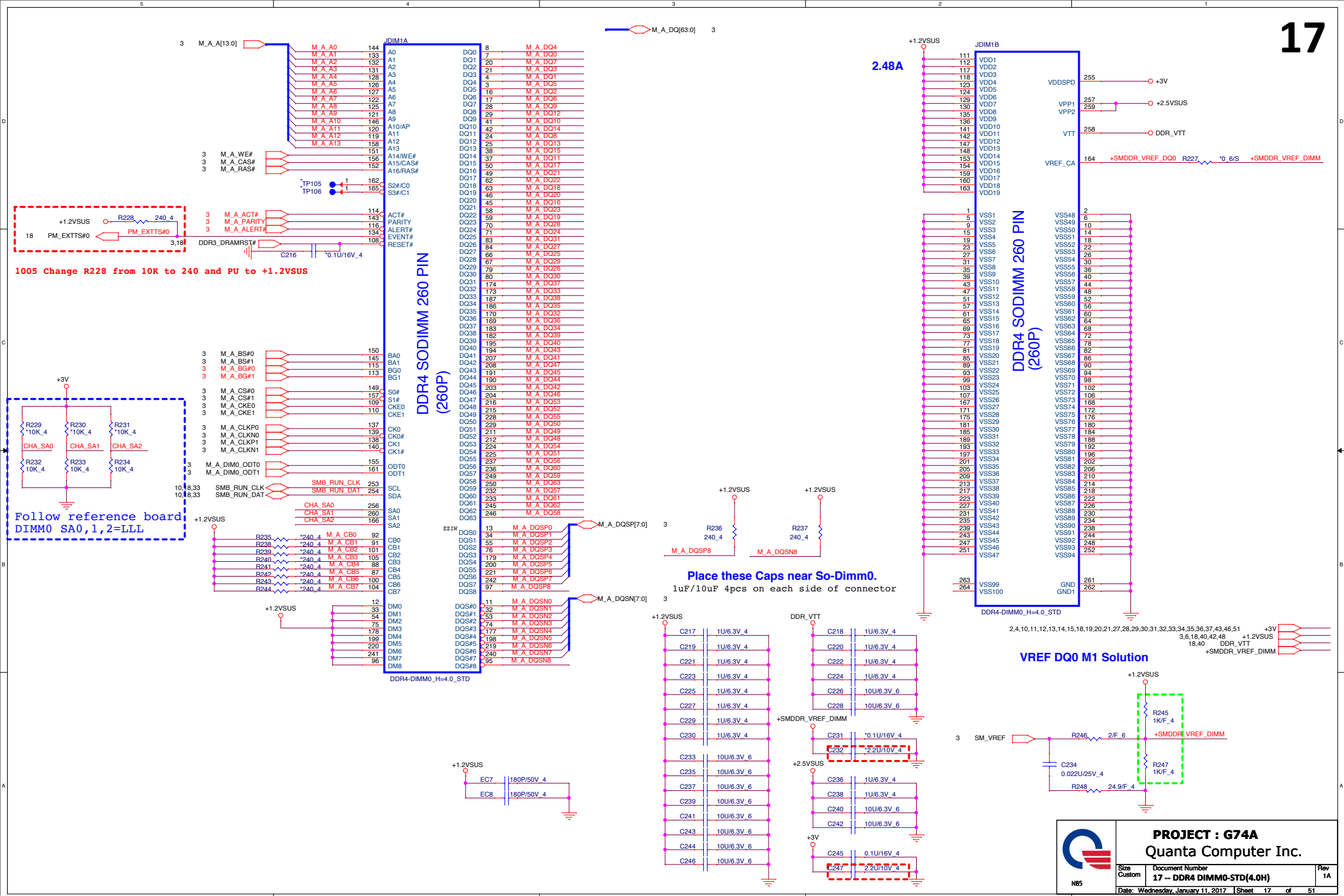
Skylake U	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 0)	0 : AMD 1 : Nvidia GPU setting	0 : 4VRAM 1 : 8VRAM	0 : VGA CAM 1 : IR CAM	00 : 14" 01 : 15 1SPD 10 : 17" 11 : 2SPD	0 : UMA 1 : DIS



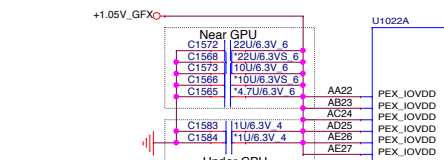




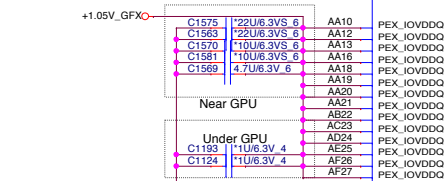




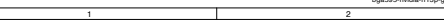
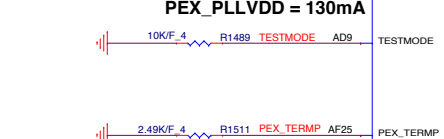
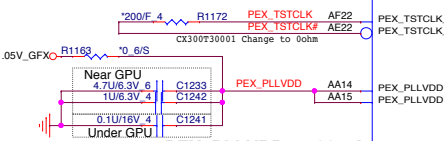
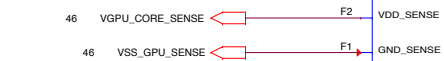
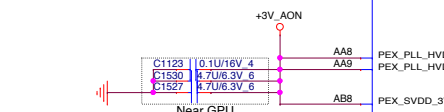


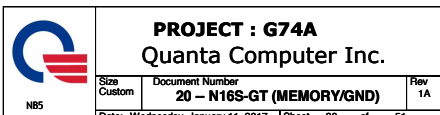


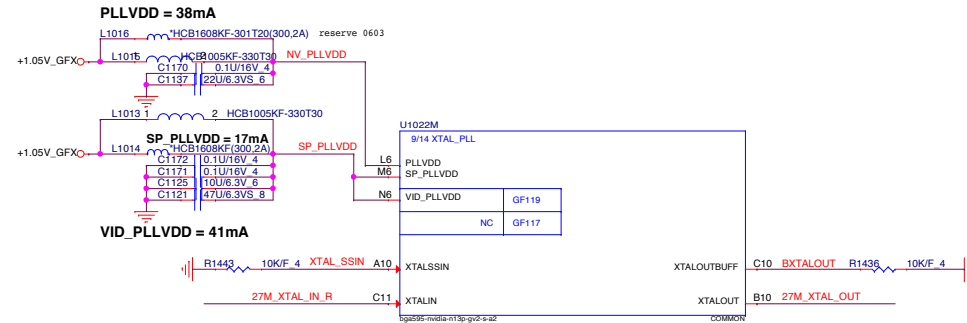
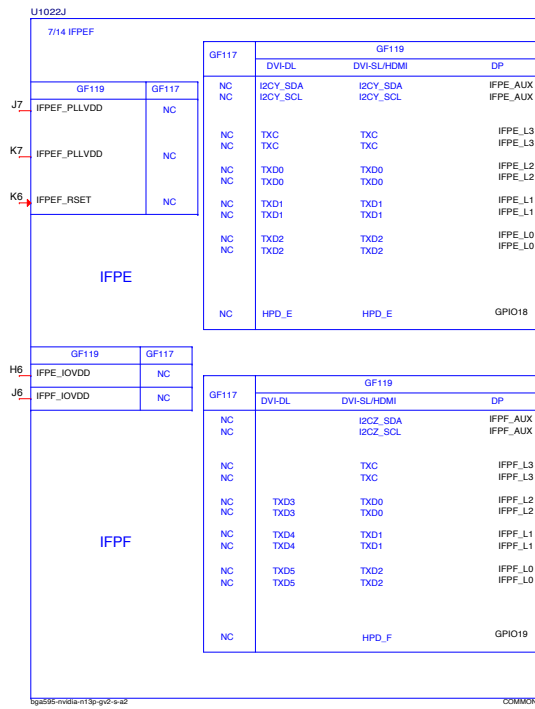
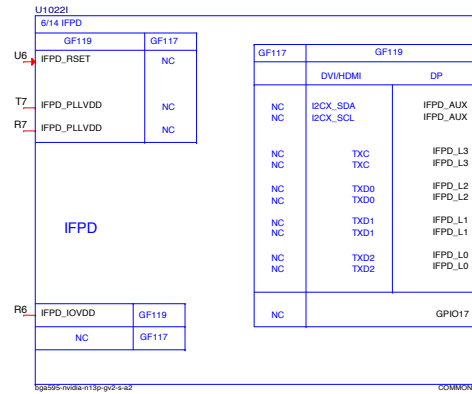
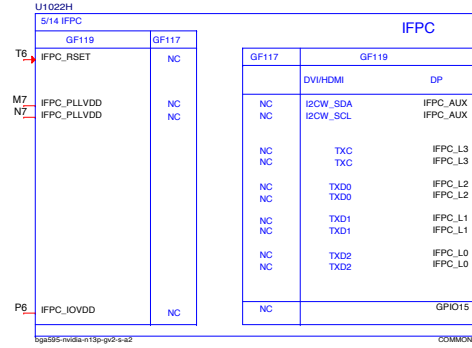
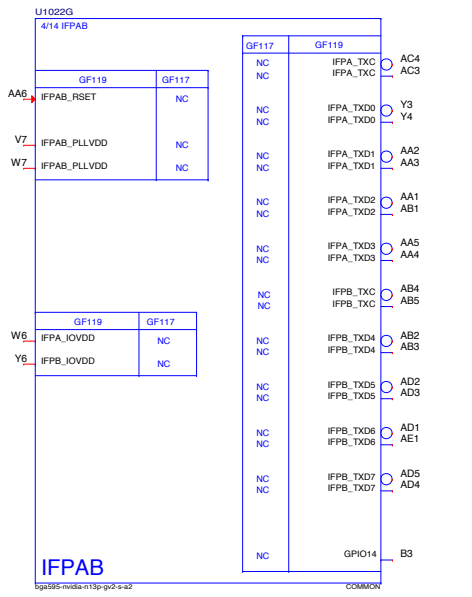
**PEX\_IOVDD + PEX\_IOVDDQ = 1.042A**



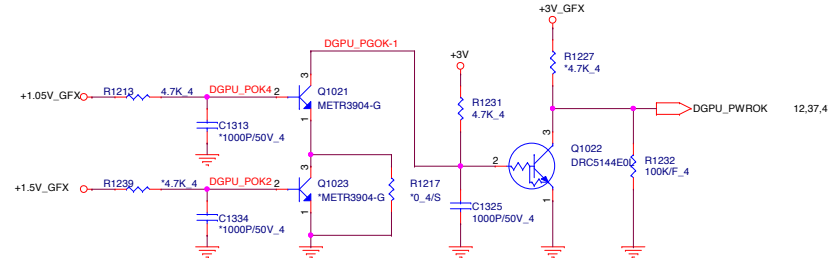
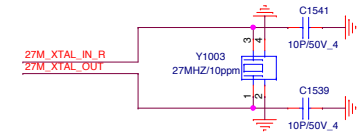
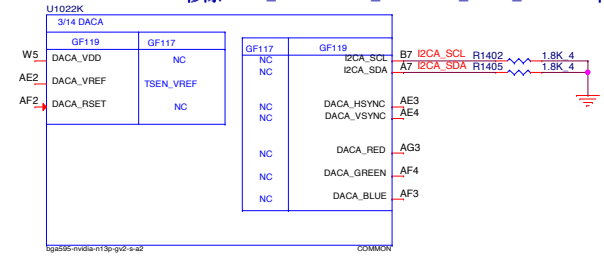
**PEX\_PLL\_HVDD + PEX\_SVDD\_3V3 = 143mA**







移除I2CA\_SDA/ I2CA\_SCL MIN\_LINE\_WIDTH 内的数值。



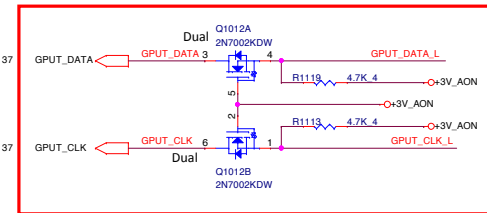
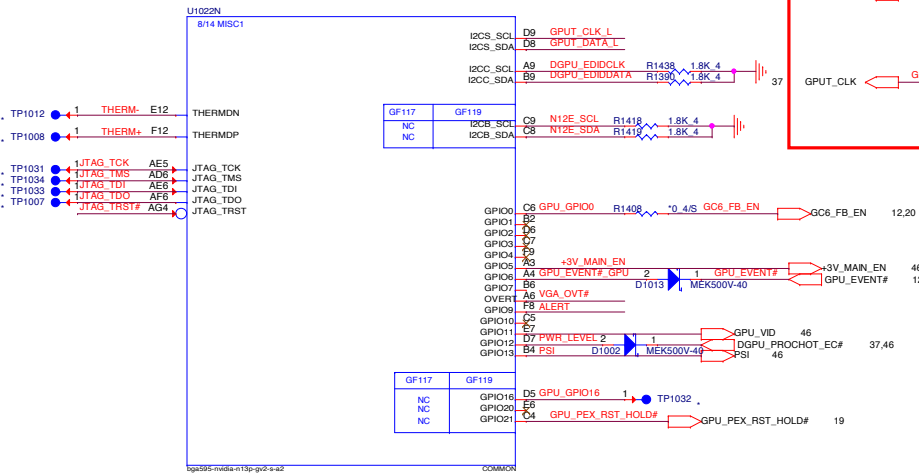
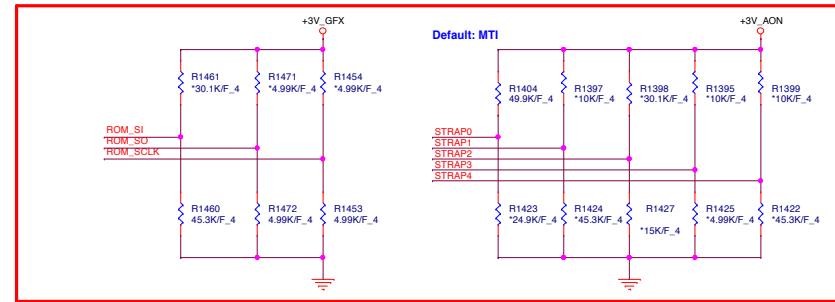
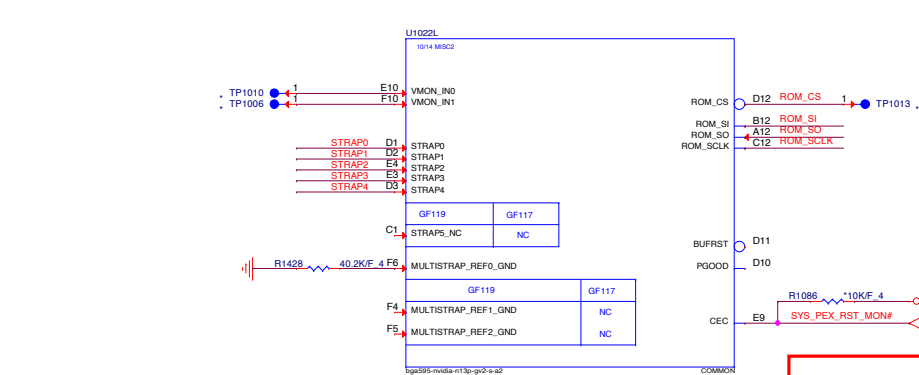


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

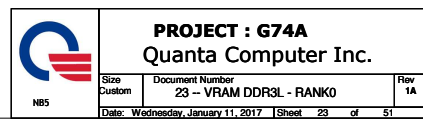
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S
1100	DDR3 256Mx16, 64bit, 4Gb, 1GMHz	HYNIX	H5TC4G63CFR-N0C	0xC	0x9	AKD5P2DTW02	AKD5P2DTW01
0111	DDR3 256Mx16, 64bit, 4Gb, 1GMHz	Micron	MT41J256M16LY-091G:N	0x7	0x3	AKD59GSTL01	AKD59GSTL00
1111	DDR3 256Mx16, 64bit, 4Gb, 1GMHz	SAMSUNG	K4W4G1646E-BC1A	0xD	0x4	AKD5PGDT501	AKD5PGDT500

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

R9056 \*1K\_4  
R9057 \*1K\_4  
R9058 \*1K\_4  
R9059 \*1K\_4PROJECT : G74A  
Quanta Computer Inc.Size Custom Document Number 22 - N16S-GT (GPIO/STRAPS) Rev 1A  
Date: Wednesday, January 11, 2017 Sheet 22 of 51

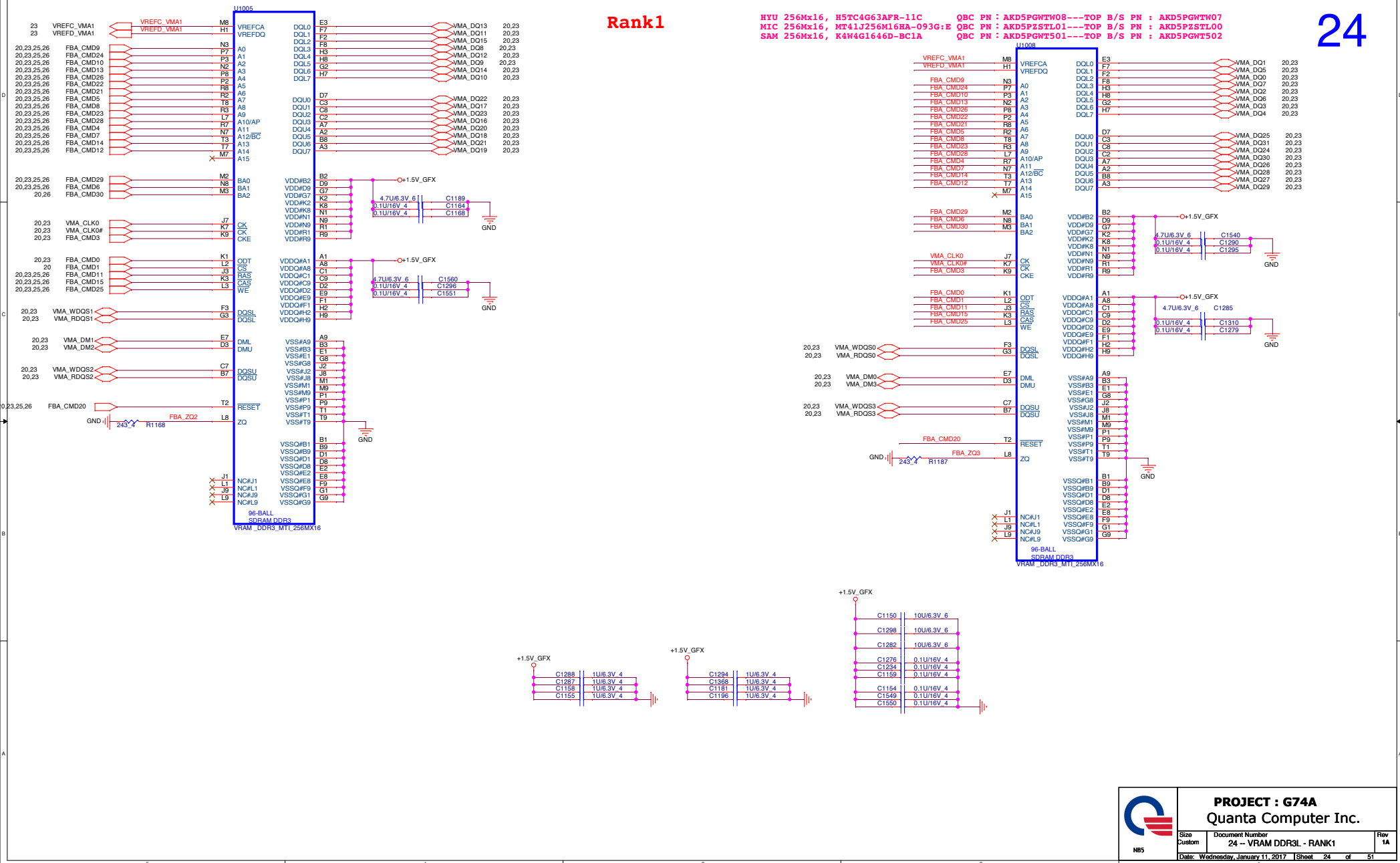




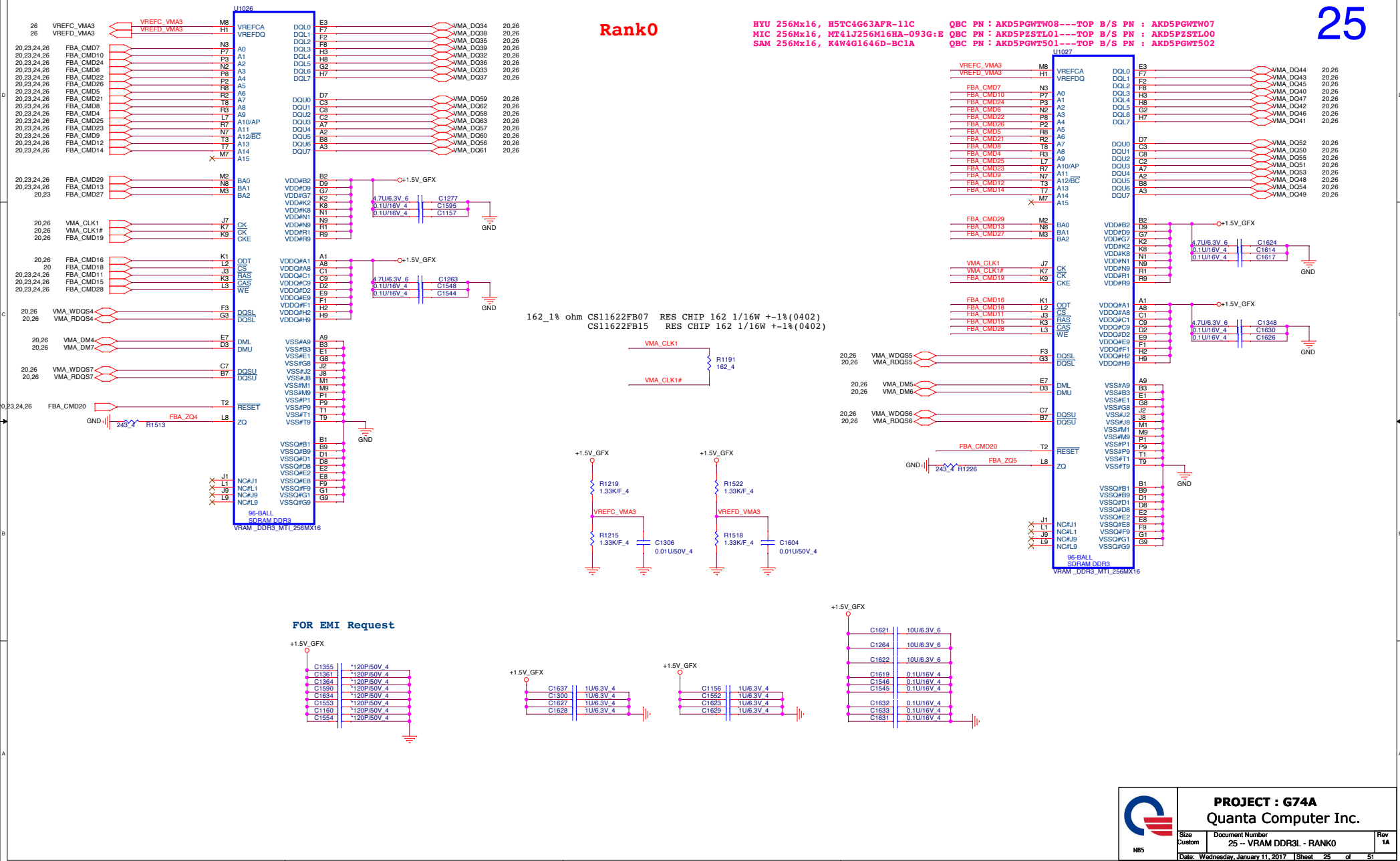
Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

24



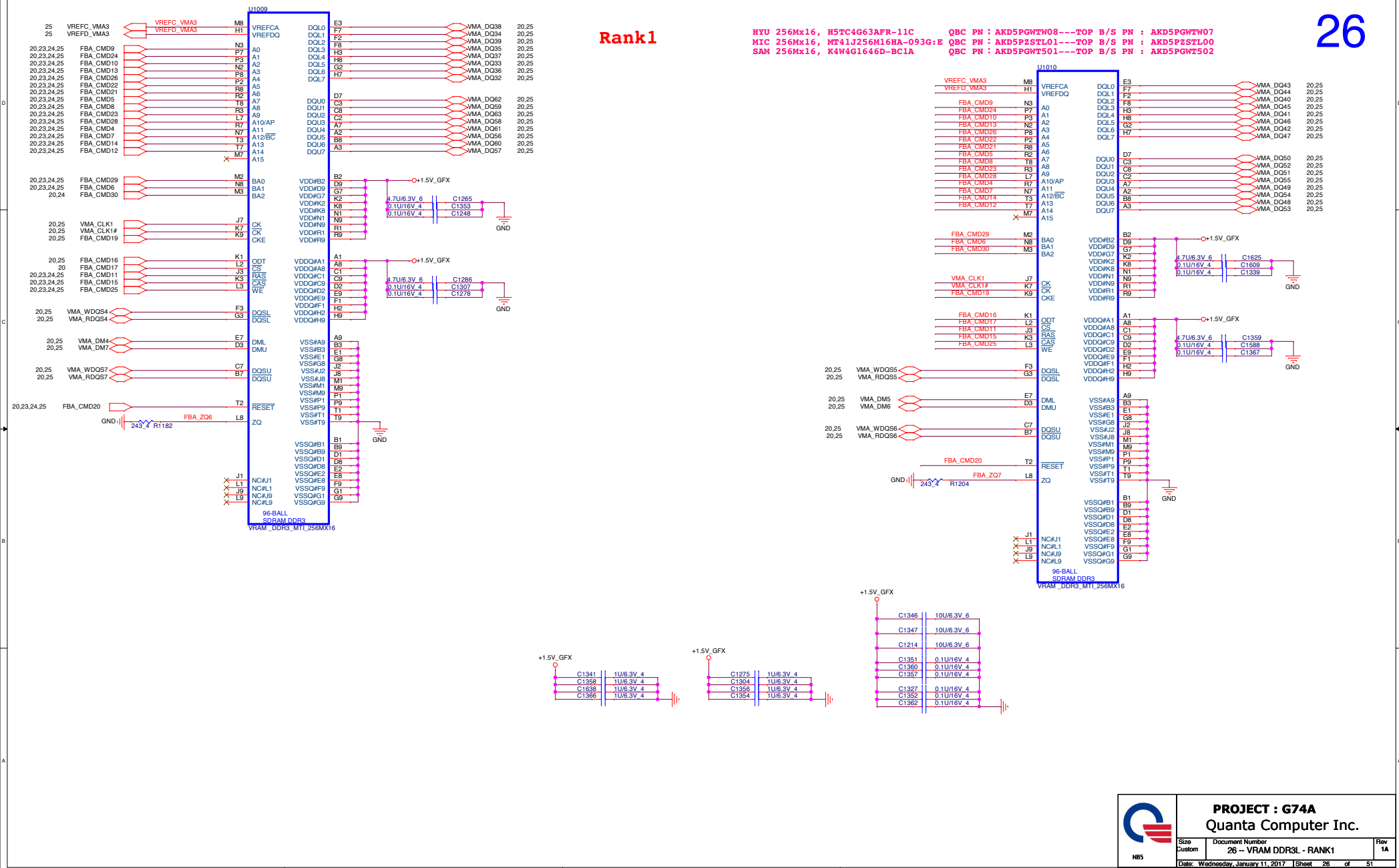




## Rank1

HYU 256Mx16, H5TC4G63AFR-11C  
MIC 256Mx16, MT41J256M16HA-093G:E  
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



7 EMU\_LID

R4501

PN\_BLOK

D4501

BLON\_CON

R4502

100K/F\_4

22P/50V\_4

LVDS\_BLOK1

R4503

1K/F\_4

LVDS\_BLOK1

R4504

100K/F\_4

2A / 80mils

+VIN\_BLIGHT

+VIN

FUSE SMD 1.5A 24V POLY

F4502

C4504

0.1U/25V\_4

C4505

0.01U/50V\_4

+VIN

C4508

4.7U/25V\_6

C4509

0.1U/25V\_6

C4510

0.1U/25V\_6

C4511

0.1U/25V\_6

C4512

4.7U/25V\_6

**+3.6V CAM\_IR**

**+3.6V CAM\_IR\_F**

**+5V**

**+5V\_TS**

**+3V\_TS**

**+3V\_CAM**

**+3.6V CAM\_IR**

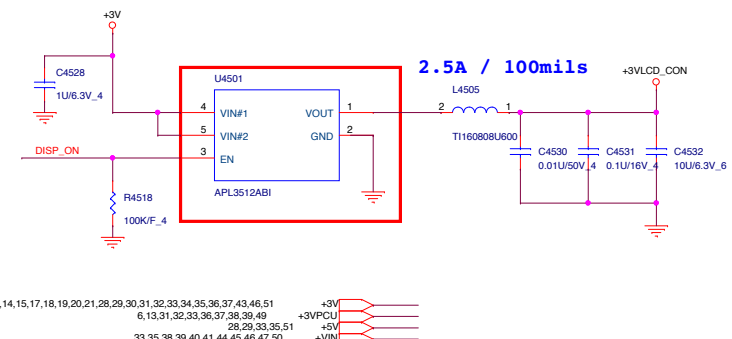
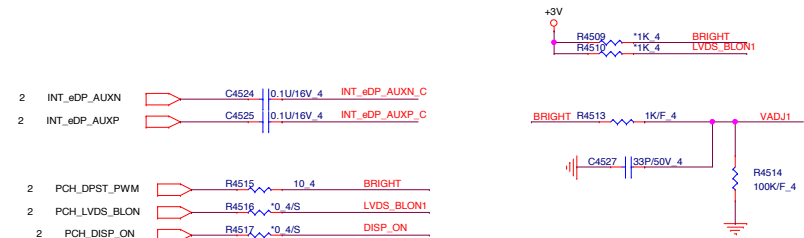
**TDC:1A**

**EDP:2A**

**VO=(0.6(R1+R2)/R2)**

**+3.6V +/- 5%**  
**TDC:1A**  
**EDP:2A**

$$V_O = (0.6(R_1 + R_2)/R_2)$$

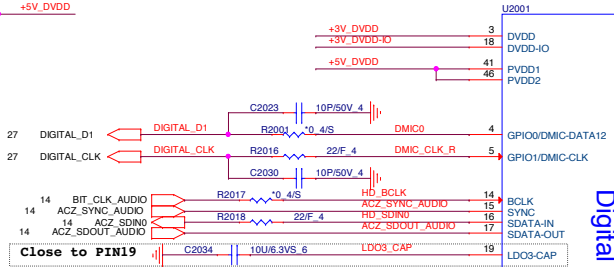
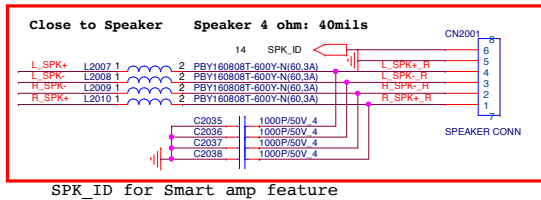
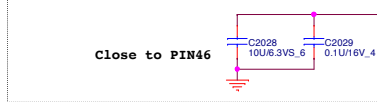
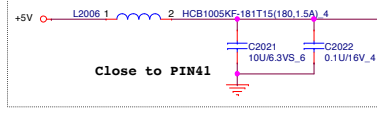
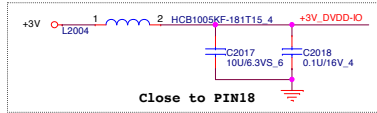
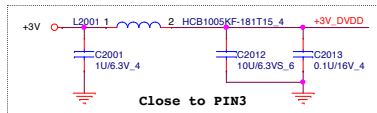


2,4,10,11,12,13,14,15,17,18,19,20,21,28,29,30,31,32,33,34,35,36,37,43,46,51 +3V  
6,13,31,32,33,36,37,38,39,49 +3VPCU  
28,29,33,35,51 +5V  
33,35,38,39,40,41,44,45,46,47,50 +VIN

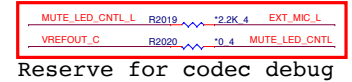
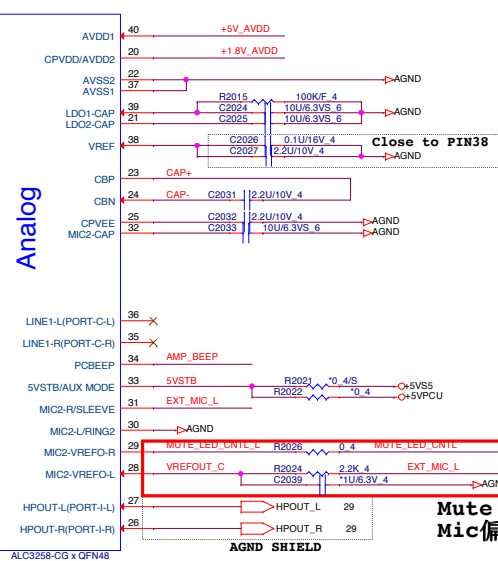


**PROJECT : G74A**  
Quanta Computer Inc.

Size Custom	Document Number 27 -- eDP CONN/LID/CAM/D-MIC/TS	Re
Date: Wednesday, January 11, 2017	Sheet 27 of 51	

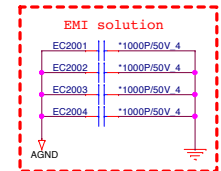
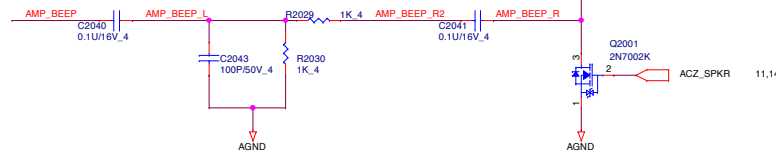
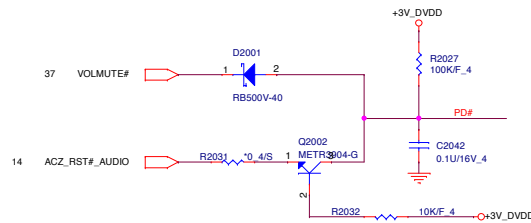
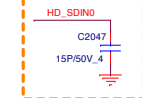


Analog



Mute LED改用Mic2-Vrefo-R  
Mic偏壓改用Mic2-Vrefo-L

Add cap for RF issue



place to under codec



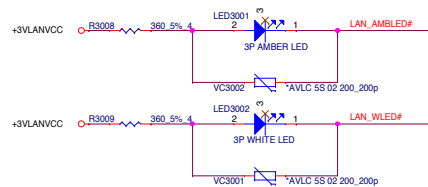
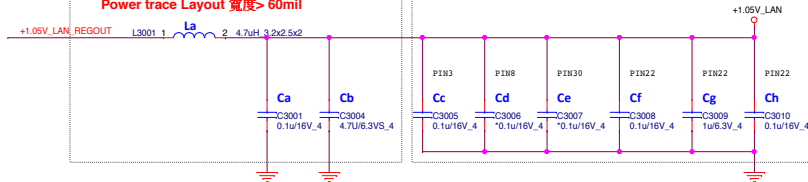


For SWR mode support  
RTL8107ESH-CG/RTL8111HSH-CG  
Stuff: La, Ca, Cb

\* Place Ca, Cd, Ce, Cf for RTL8107ESH-CG/RTL8111HSH-CG  
close to each VDD10 pin-- 3, 22, 8, 30

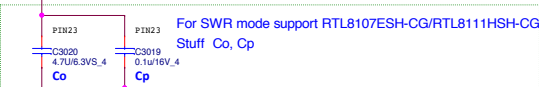
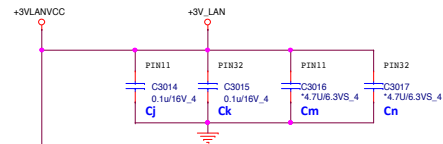
\* Place Cg, Ch for RTL8107ESH-CG/RTL8111HSH-CG  
close to each VDD10 pin-- 22(reserved)

Power trace Layout 宽度>60mil

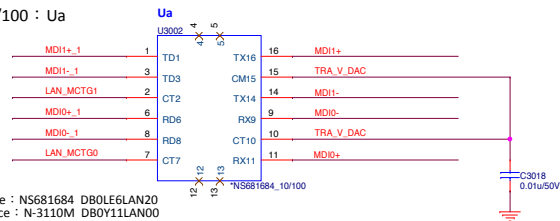


\* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for  
RTL8107ESH-CG/RTL8111HSH-CG

\* For surge improvement, place Cm and Cn, close to each  
VDD33 pin-- 11, 32(optional)

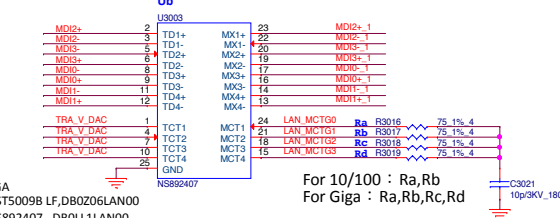


For 10/100 : Ua



1st source : NS681684 DB0LE6LAN20  
2nd source : N-3110M DB0Y11LAN00

For Giga : Ub



For GIGA  
BOT:GS75009B LF,DB0Z06LAN00  
FCE :NS892407 ,DB0LL1LAN00

For 10/100 : Ra,Rb  
For Giga : Ra,Rb,Rc,Rd

LAN\_AMBLE# → TP3001  
LAN\_LED1 → TP3002  
LAN\_LED2 → TP3003

if ISOLATEB pin pull-low,  
the LAN chip will not drive it's PCI-E outputs  
(excluding PCIE\_WAKE# pin )

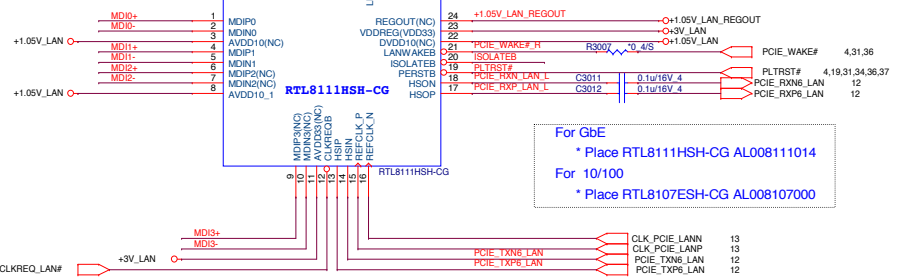
For GbE

\* Place Ra

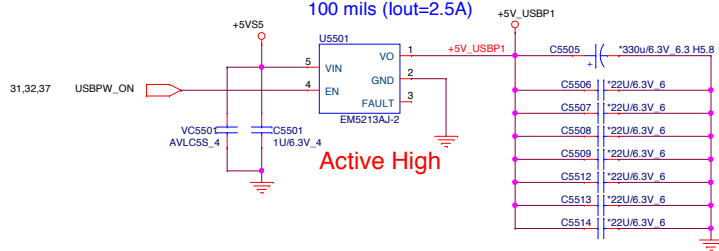
For 10/100

\* Place Rb

Add 9 GND VIAs with thermal PAD



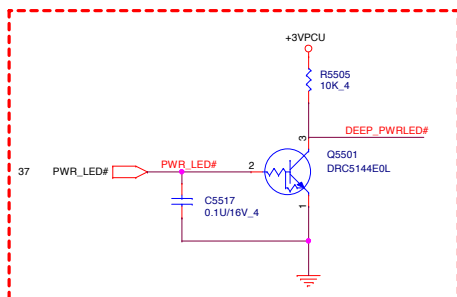
100 mils (Iout=2.5A)



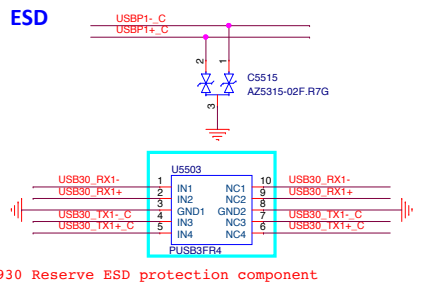
Active High

## Daughter Board

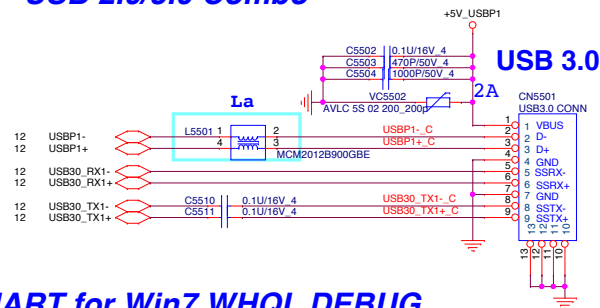
1123 Add PWR LED MOS Circuit



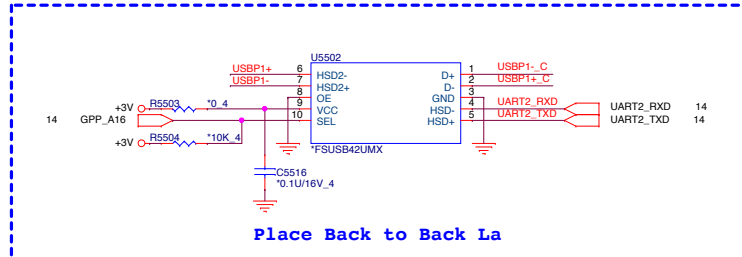
## ESD



## USB 2.0/3.0 Combo



## UART for Win7 WHQL DEBUG

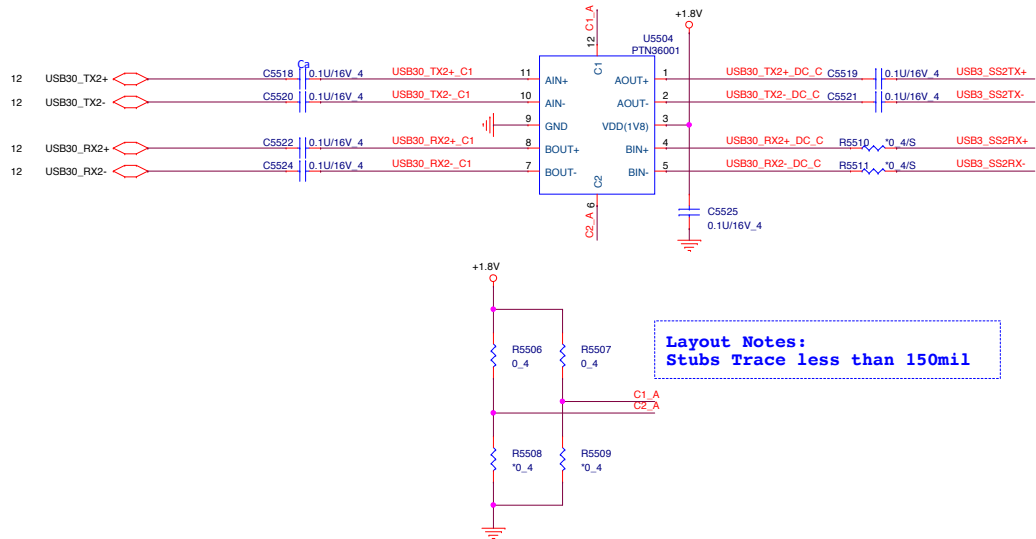


Place Back to Back La

## USB3.0

USB3.0 Re-driver IC

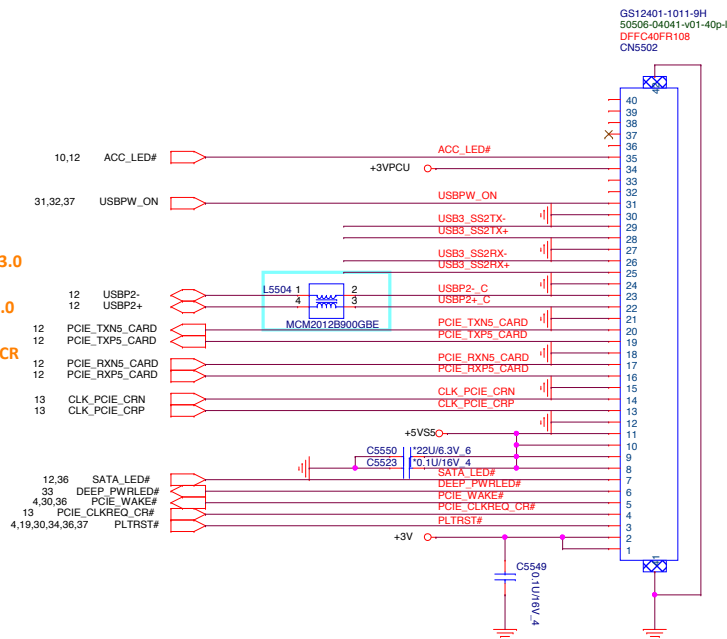
## USB3.0 re-driver IC

Layout Notes:  
Stubs Trace less than 150mil

2 SPD:1 USB3.0

2 SPD :1 USB2.0

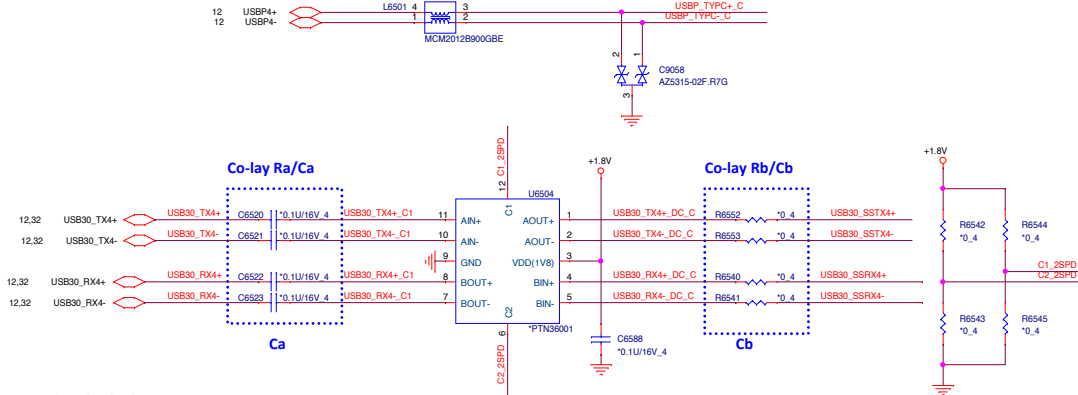
15" :PCIE to CR



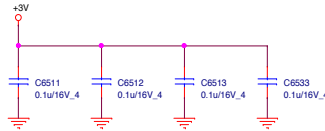
# USB3 SW - EJ179S + USB TYPE-C - TPS25810

32

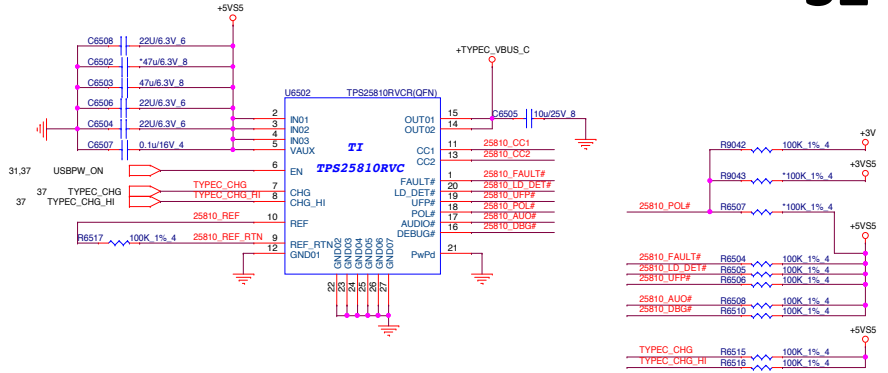
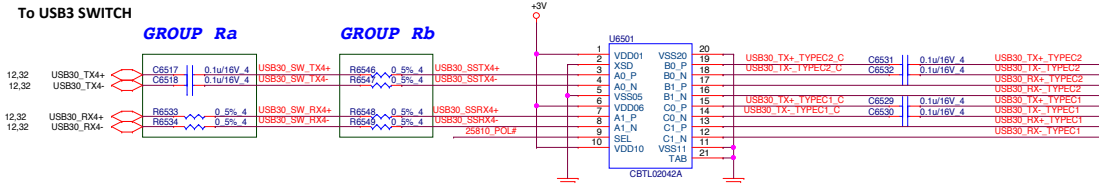
## USB2.0



## USB3.0 SW



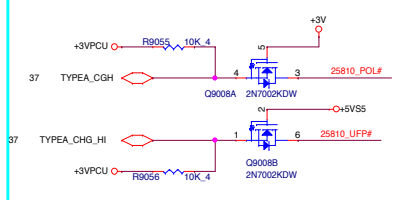
## Differential impedance referenced SOC



TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLB	UFPb	AUDIOb	DEBUb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW	Hi-Z
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

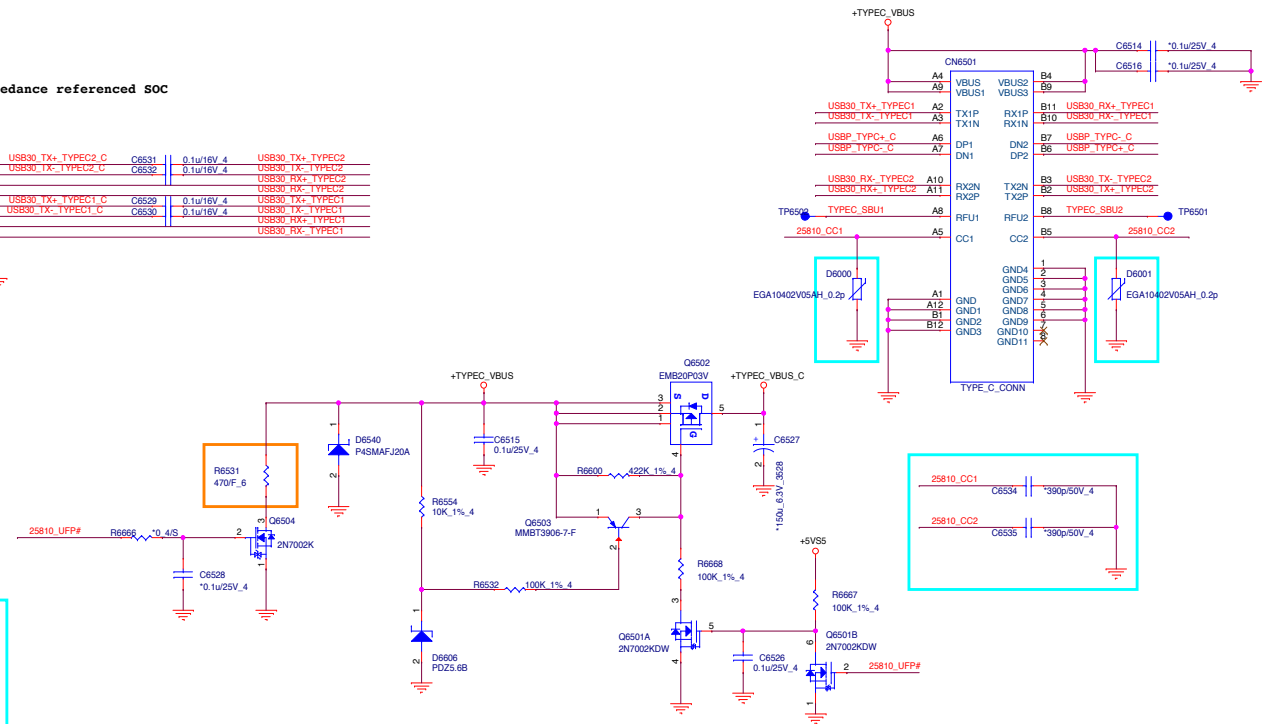
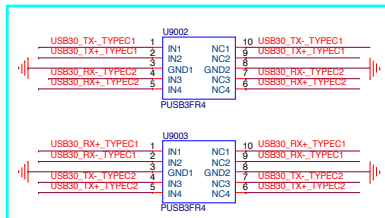
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

## Add Type-C A/B side recognition



SEL = CMOS single-ended input  
operation mode select  
SEL = LOW: A <----> B  
SEL = HIGH: A <----> C

## TYPE C USB3.0 ESD



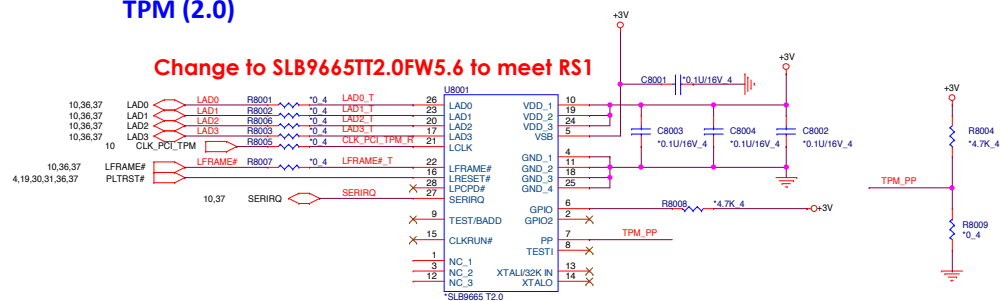


***KB LIGHT CONN***

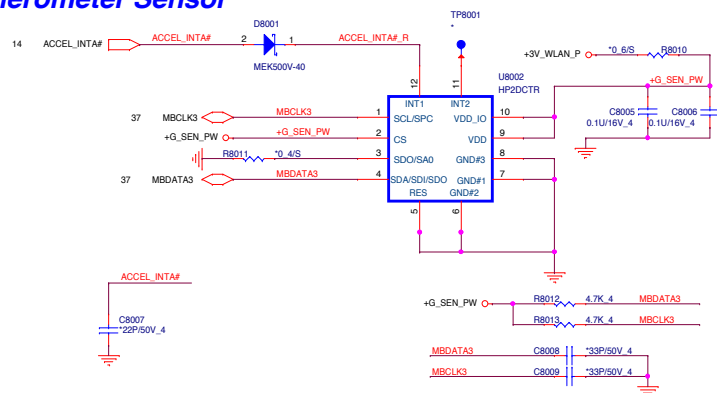


## TPM (2.0)

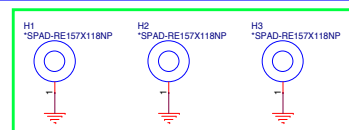
Change to SLB9665TT2.0FW5.6 to meet RS1



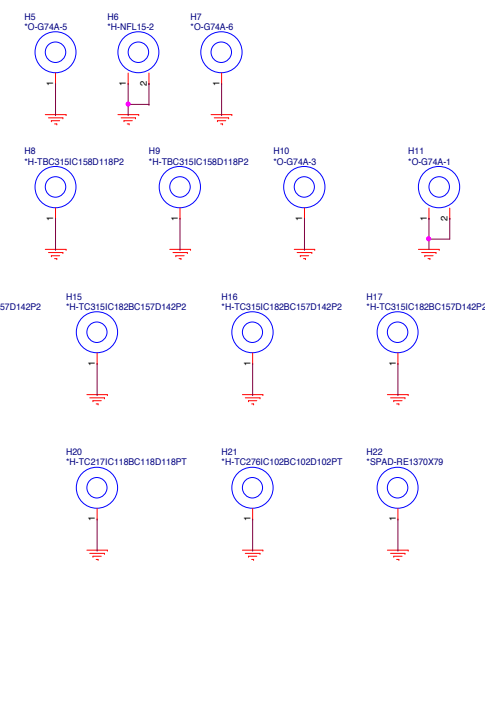
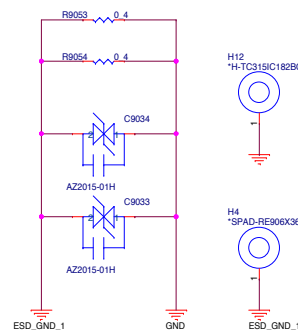
## Accelerometer Sensor



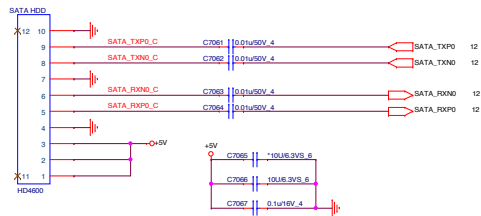
## Holes



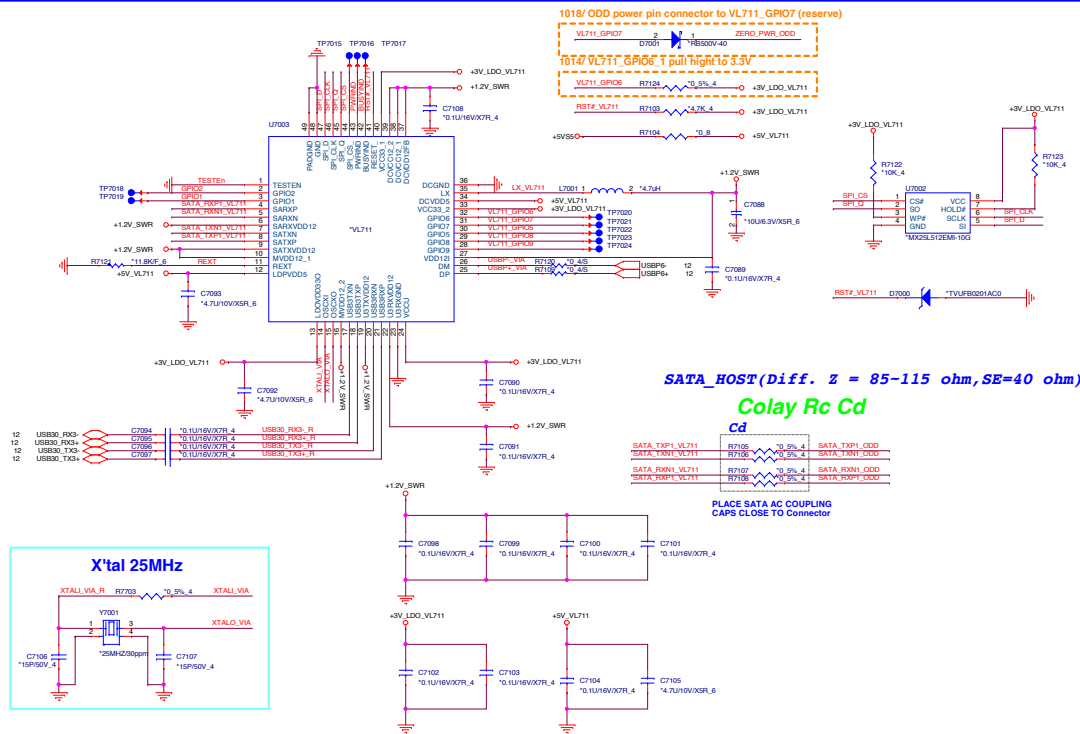
10/17 EMI request



# SATA HDD & LED

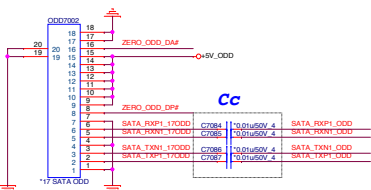


# USB3.0 to SATA

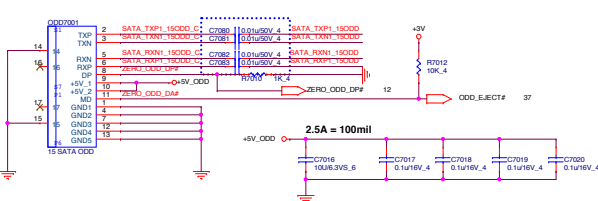


# SATA ODD

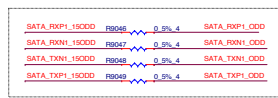
17.3" ODD



15.6" ODD

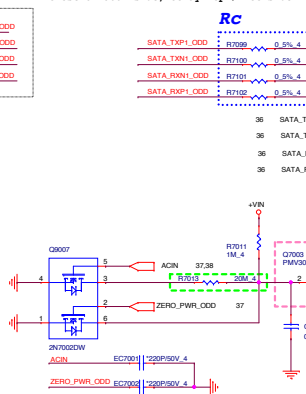


Colay Cc, Ce  
15.6" ODD STUFF



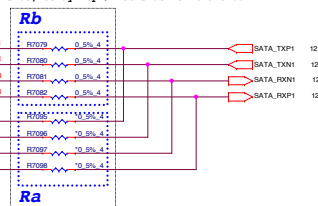
Colay Rc, Cd

Close ODD7001 side, Colay Top / Bot side for branch!!



Colay Ra, Rb

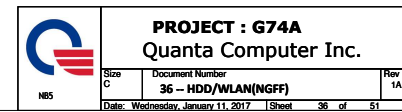
Close CPU side, Colay Top / Bot side for branch!!

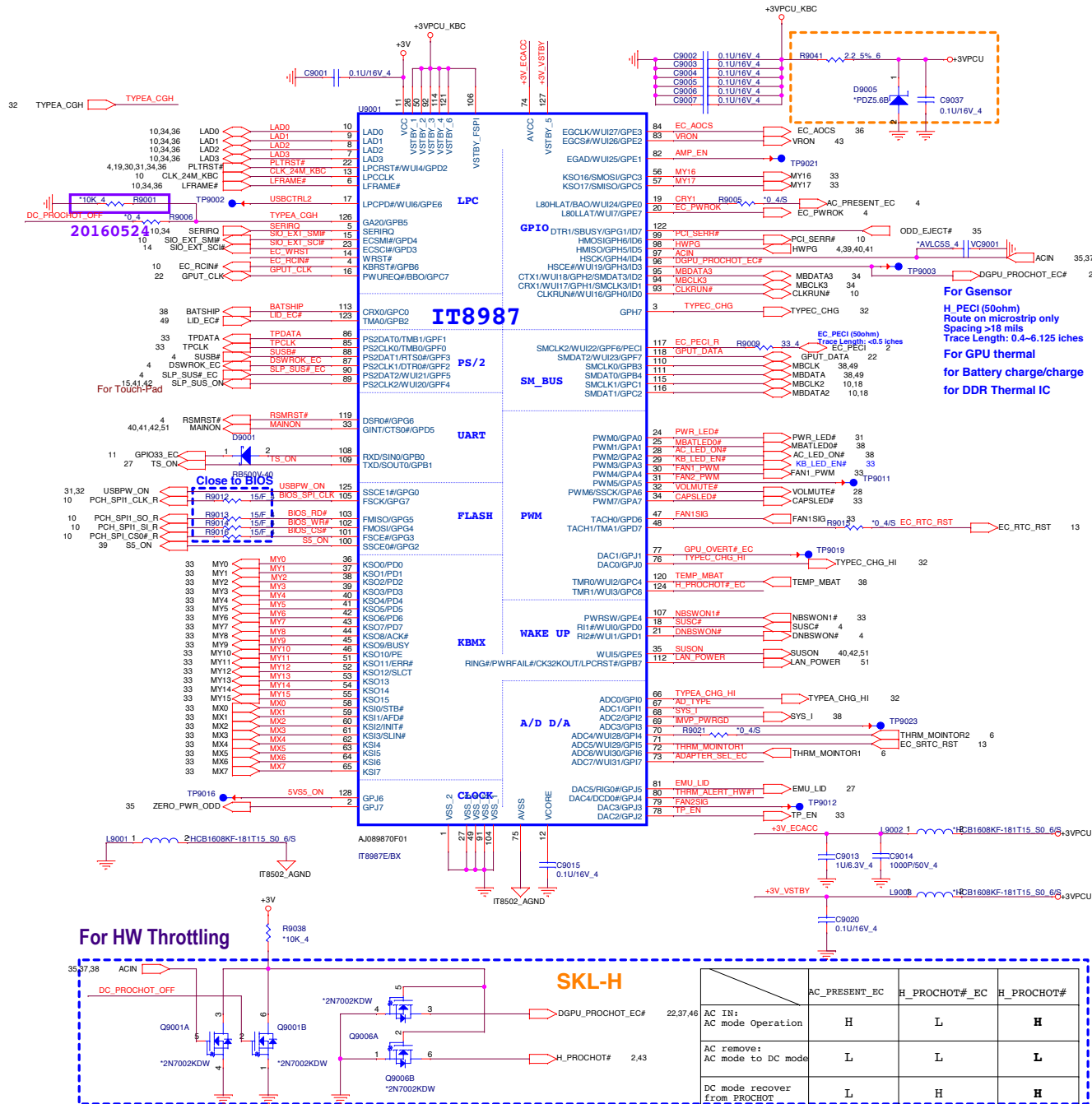


High : ODD power down  
Low : ODD power on



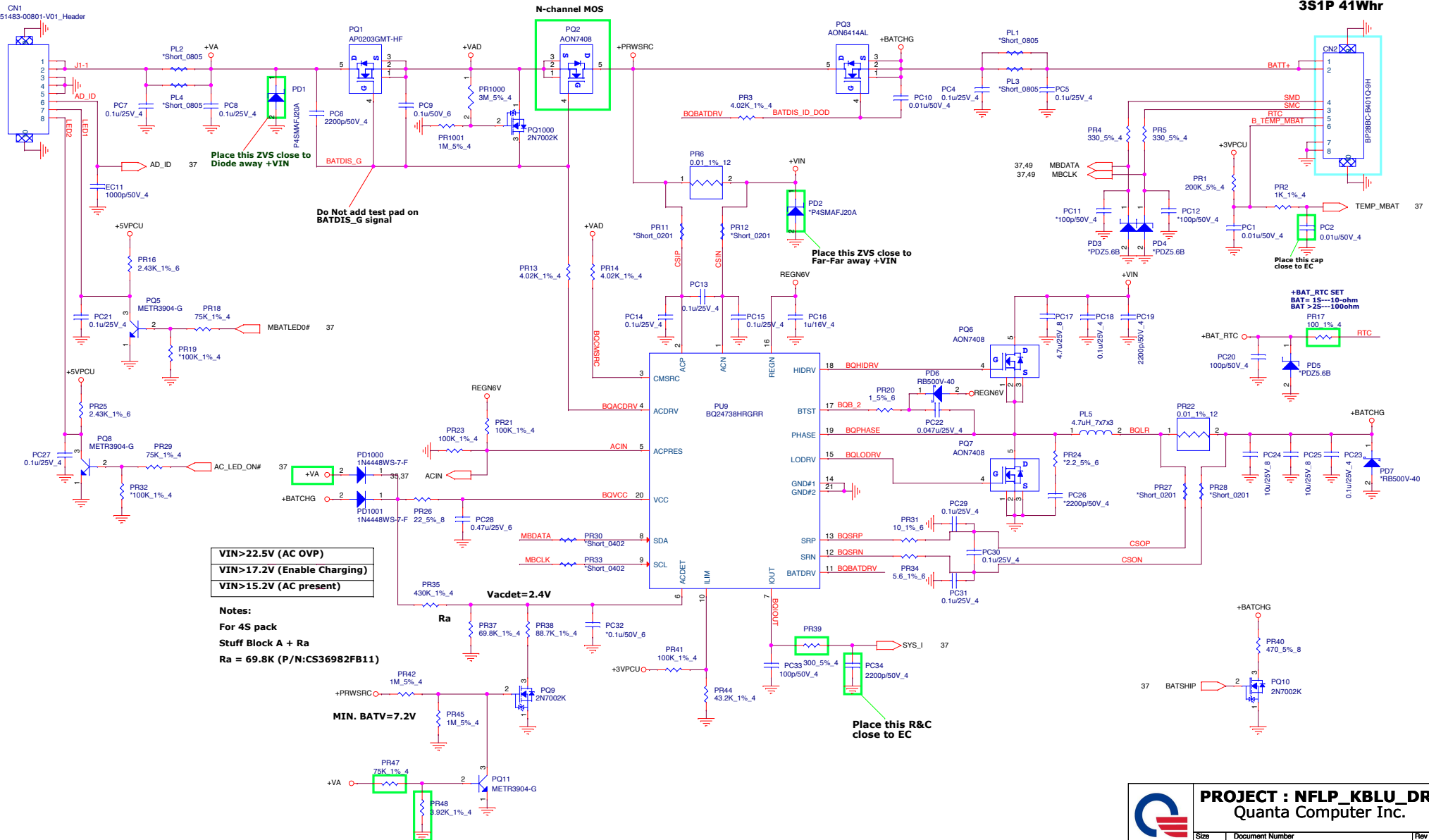
# WLAN



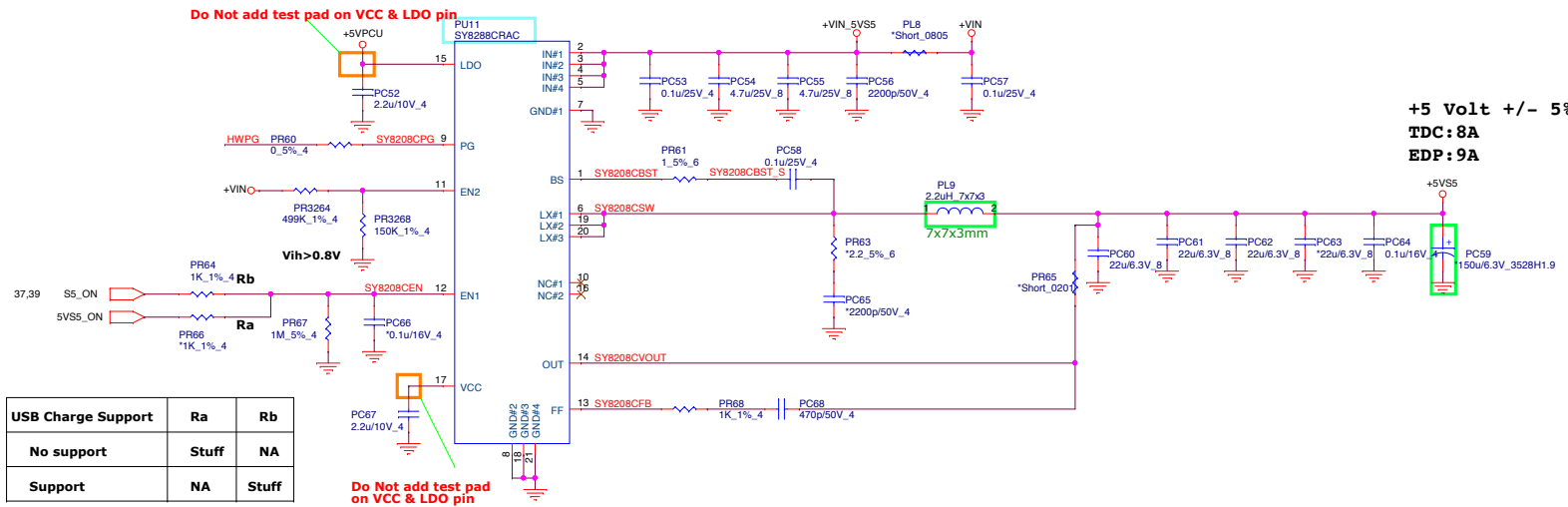
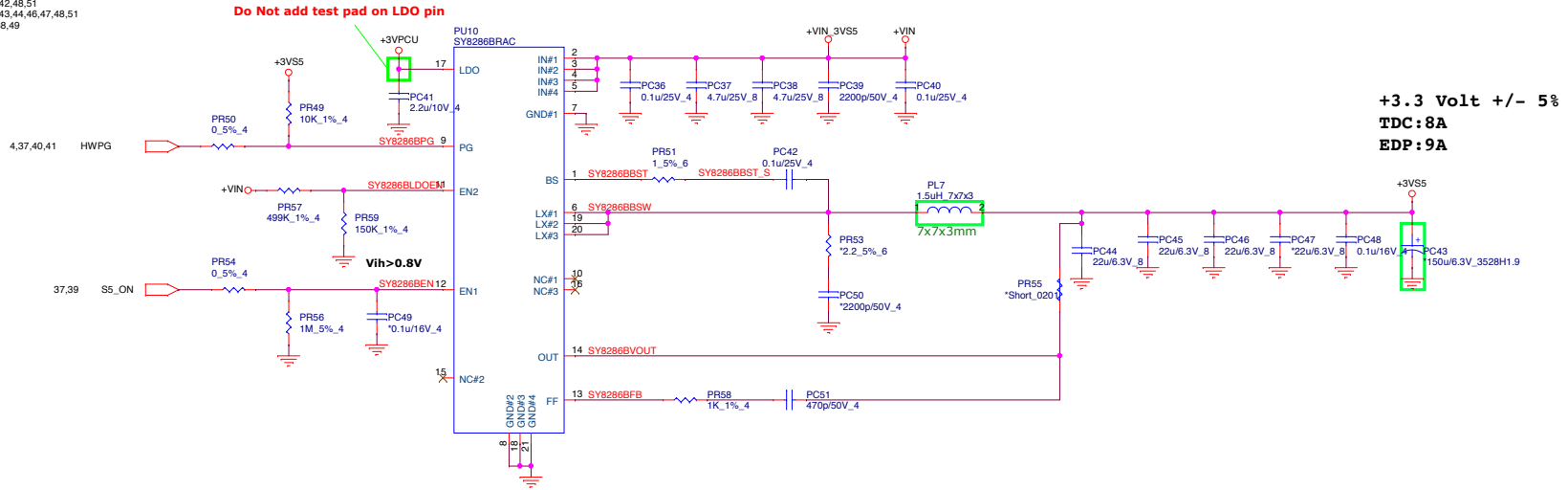


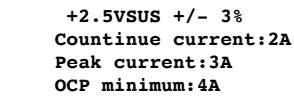
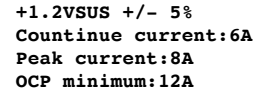
+3VPCU	6,13,31,32,33,36,37,38,39,49
+5VPCU	28,39,48,51
+BAT_RTC	4,13,15,33,49
+VIN	27,33,35,39,40,41,44,45,46,47,50
+3VPCU	6,13,31,32,33,36,37,38,39,49

## ADP=65W



+VIN	27,33,35,38,40,41,44,45,46,47,50
+3VS5	4,10,15,32,36,37,40,41,42,48,51
+5VS5	4,28,31,32,35,40,41,42,43,44,46,47,48,51
+3VPCU	6,13,31,32,33,36,37,38,49
+5VPCU	28,38,48,51



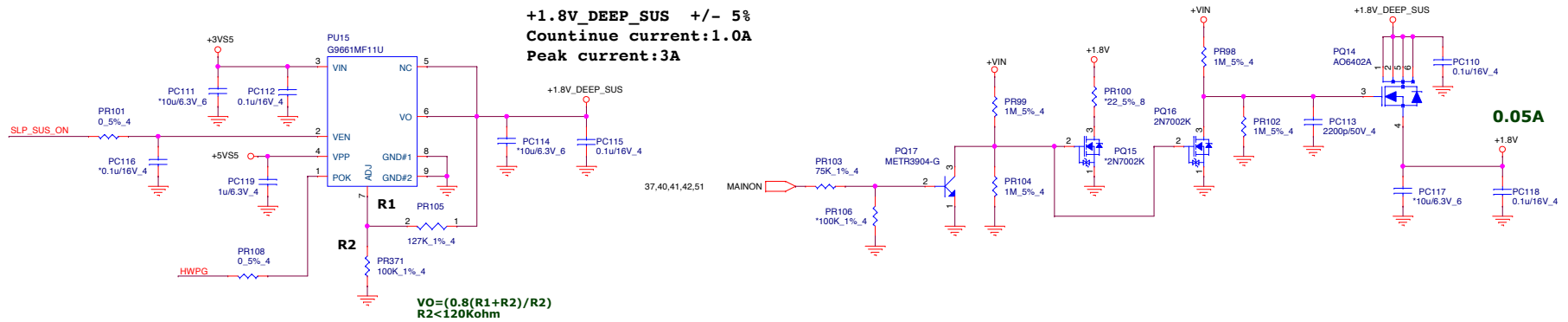
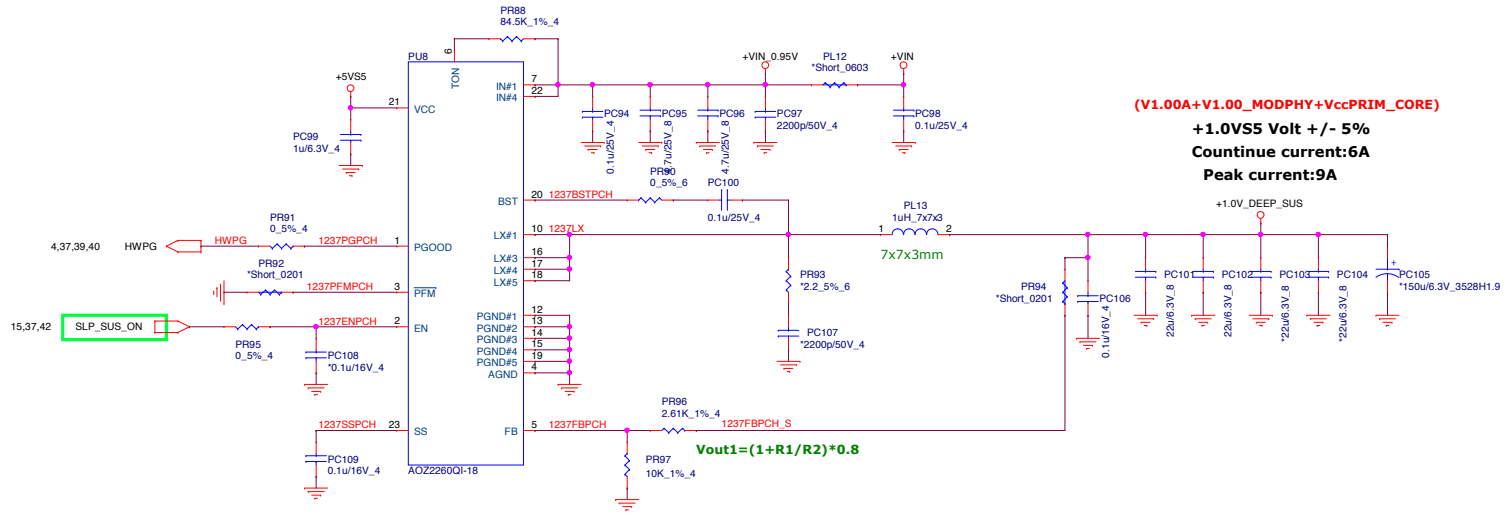


$$V_O = (0.8(R_1 + R_2)/R_2)$$

$$R_2 < 120 \text{ Kohm}$$



+VIN	27,33,35,38,39,40,44,45,46,47,50
+3VS5	4,10,15,32,36,37,39,40,42,48,51
+5VS5	4,28,31,32,35,39,40,42,43,44,46,47,48,51
+1.0V_DEEP_SUS	9,13,15,42
+1.8V_DEEP_SUS	9,15
MAINON	37,40,41,42,51
+1.5V	

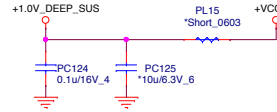


+1.0V	2,4,6,37
+3VSS	4,10,15,32,36,37,39,40,41,48,51
+5VSS	4,28,31,32,35,39,40,41,43,44,46,47,48,51
+VCCIO	2,6
+1.2V_SUS	3,8,17,18,40,48
+VCCSTPLL	2,4,5,6,9,43
+1.0V_DEEP_SUS	9,13,15,41
+1.2V_VCCPLL_OC	6
MAINON	37,40,41,51

**Volume Segment**  
**Vcc\_ST: 0.12A**  
**Vcc\_PLL: 0.12A**

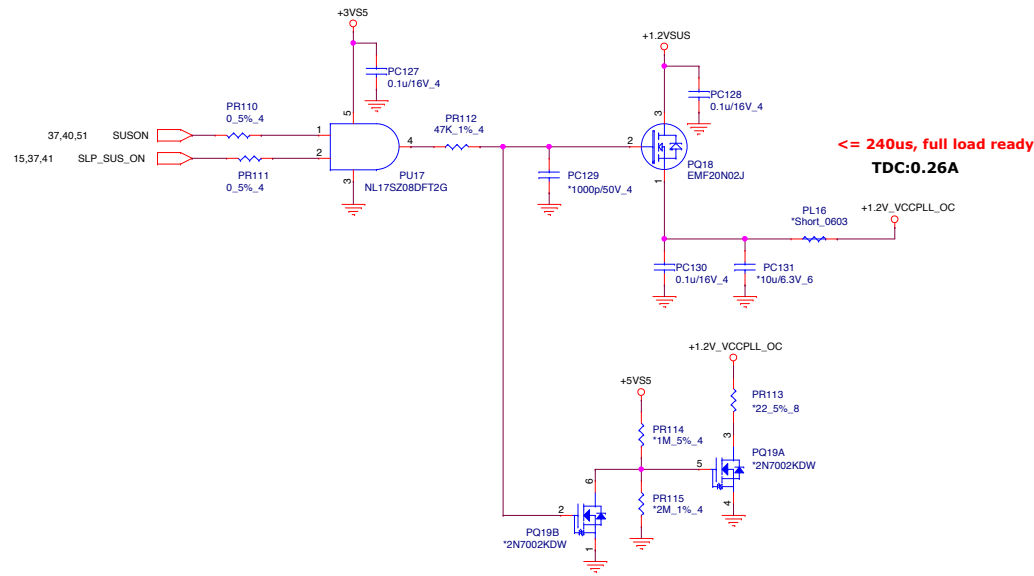
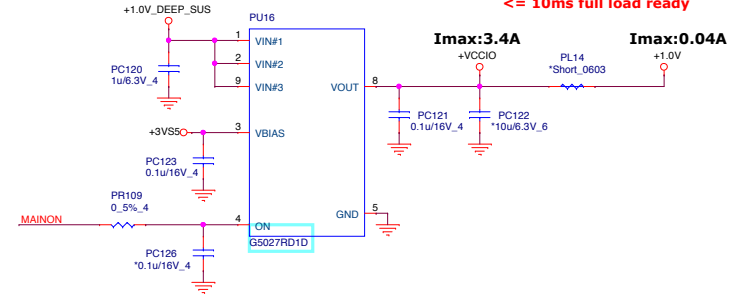
**<= 10ms, full load ready**  
**(Vcc\_ST+Vcc\_PLL)**

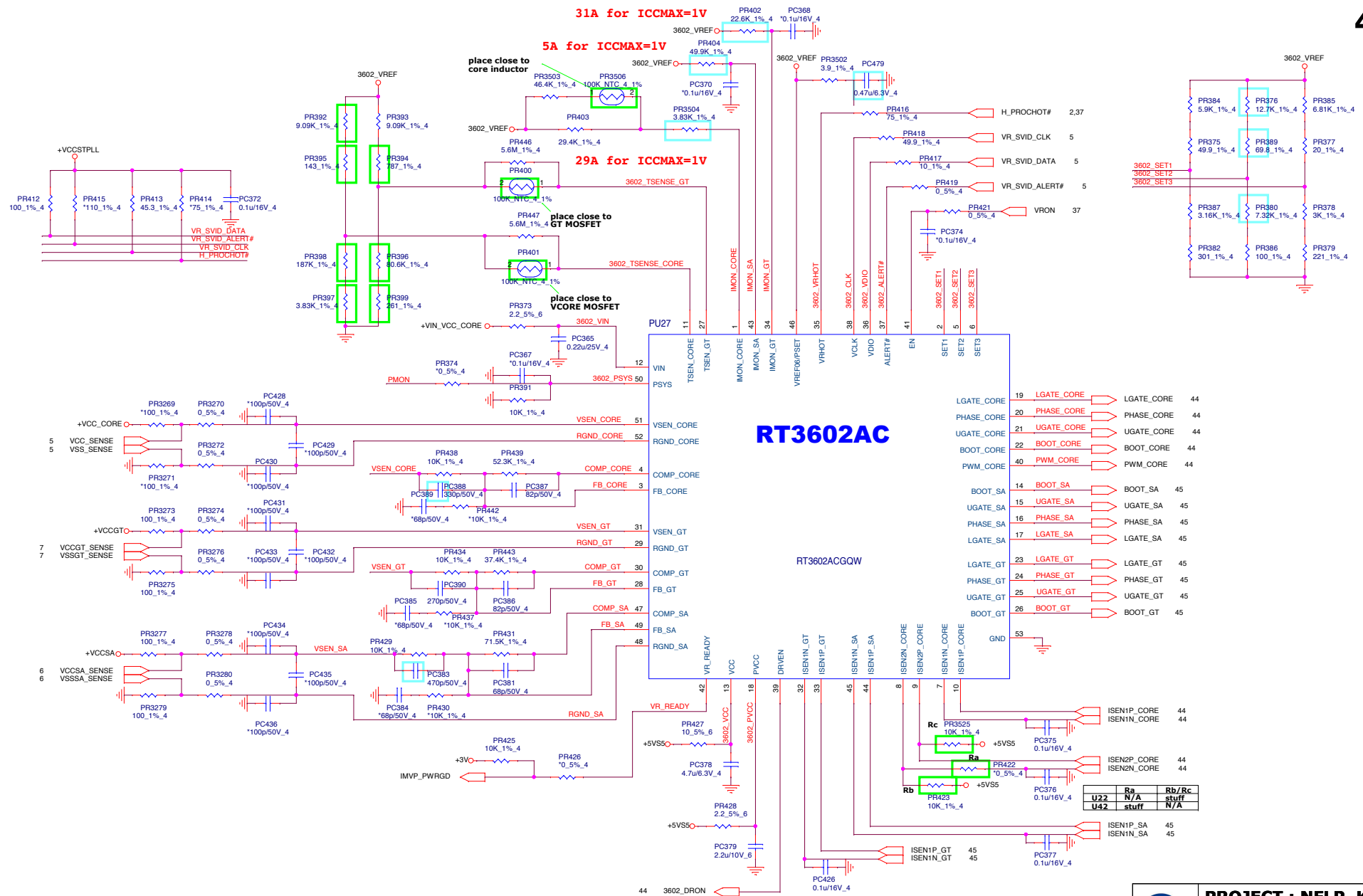
**Imax:0.24A**



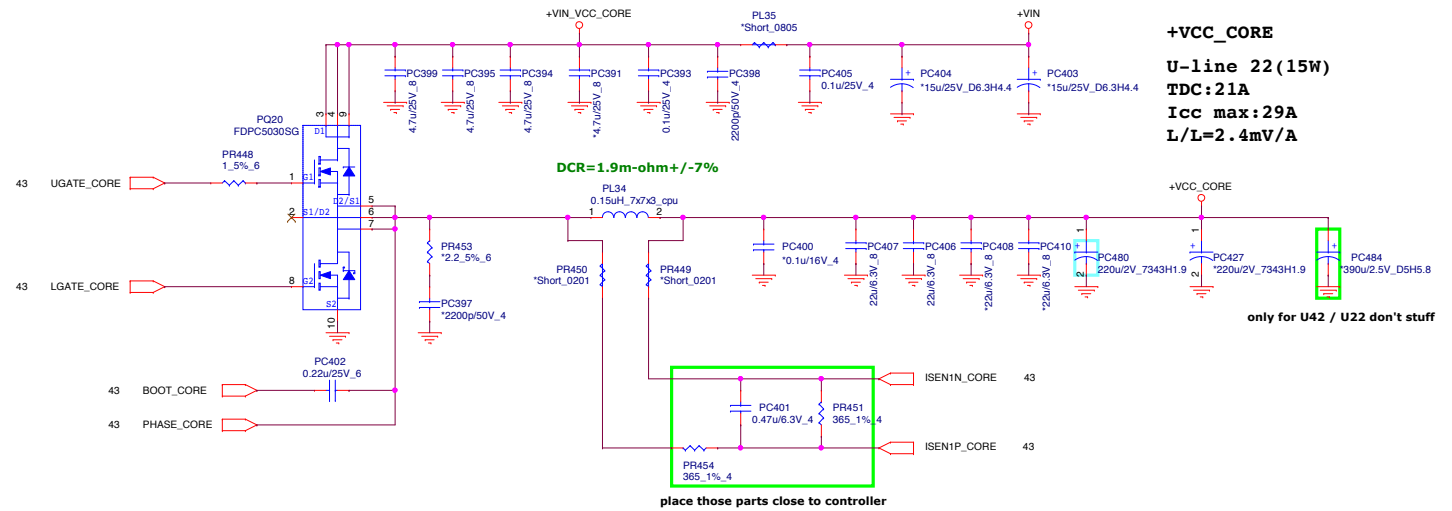
**Volume Segment**  
**Vcc\_STG: 0.04A**  
**Vcc\_IO: 3.4A**

**<= 10ms full load ready**

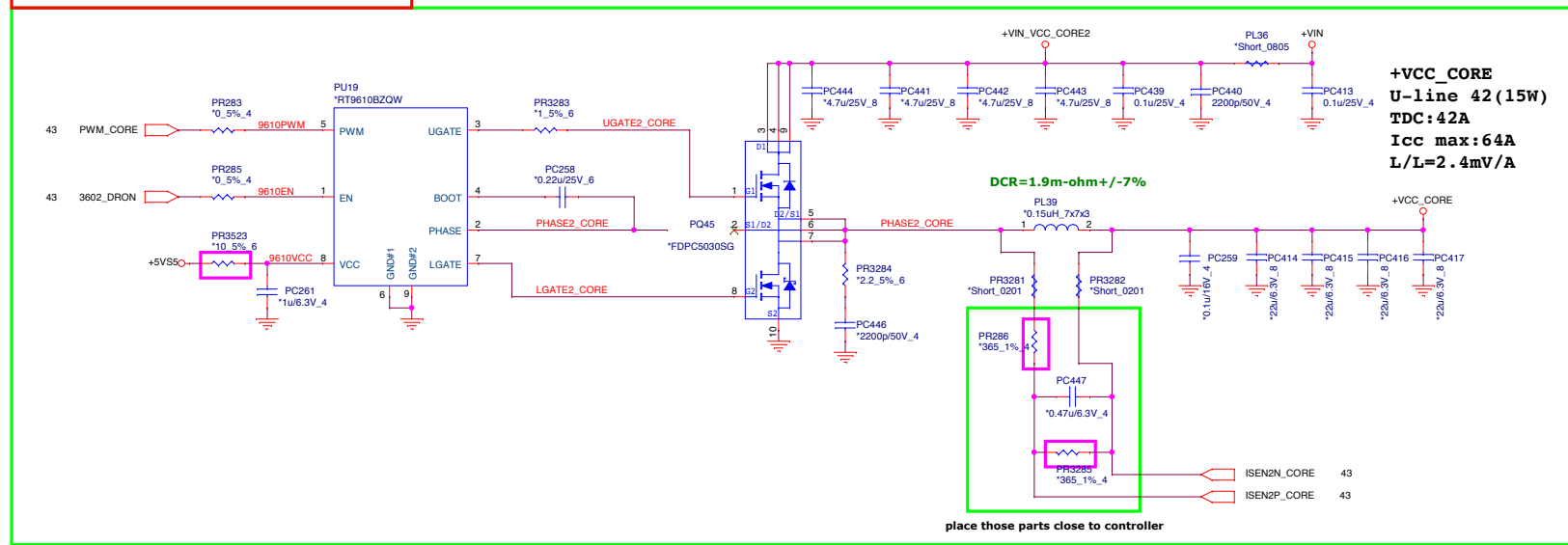




+VIN 27,33,35,38,39,40,41,45,46,47,50  
+5VSS 4,28,31,32,35,39,40,41,42,43,46,47,48,51



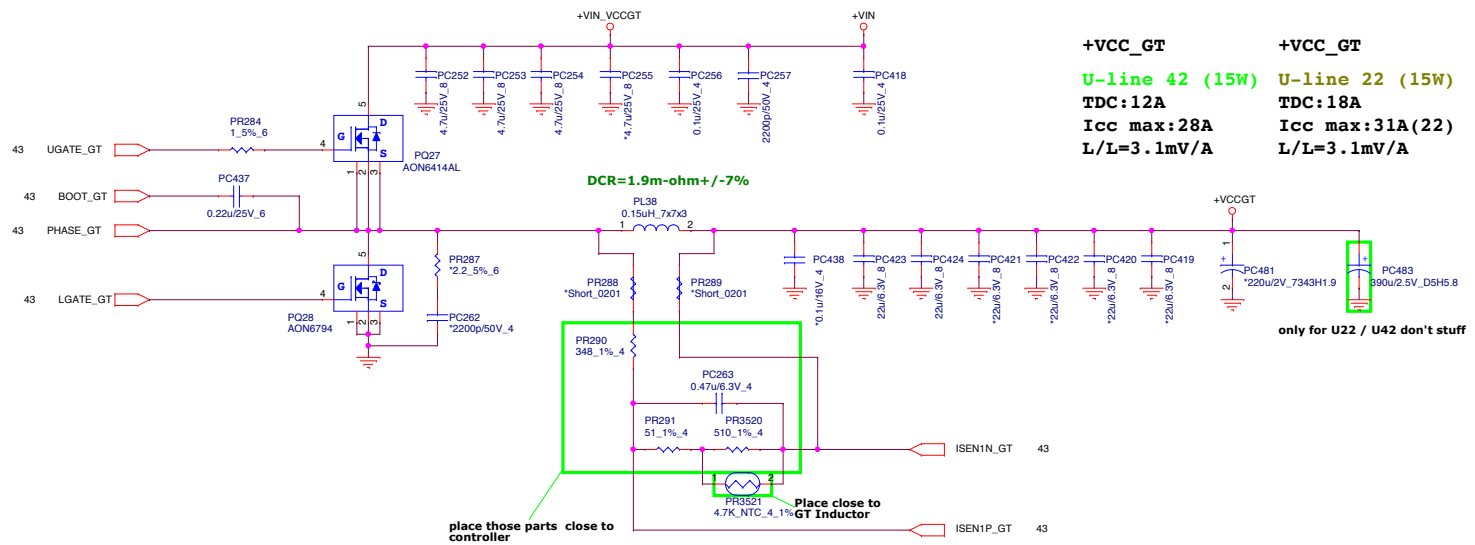
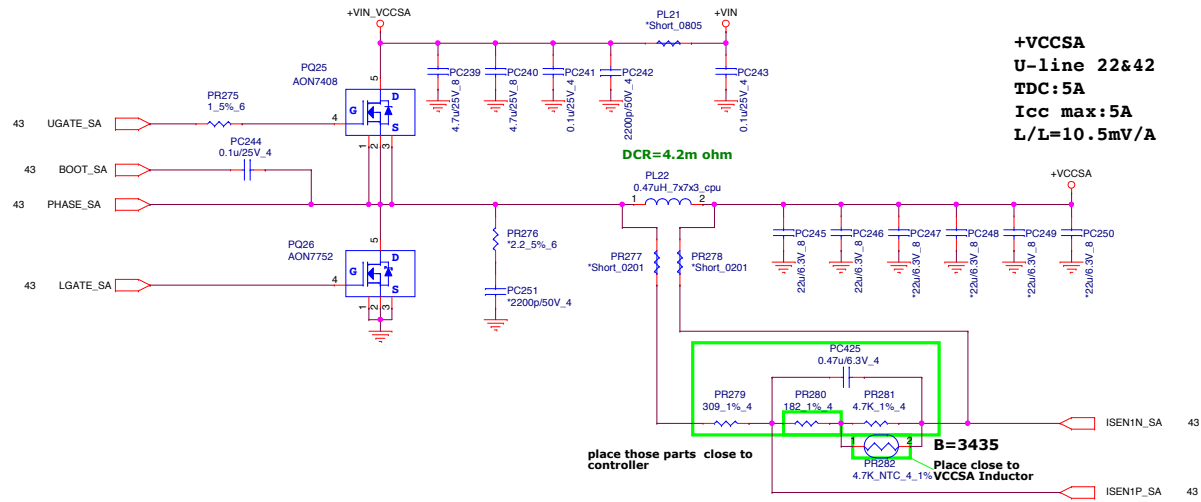
For U42 --> Add These Components



**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

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Date:	Wednesday, January 11, 2017	Sheet 44 of 51

+VIN	27,33,35,38,39,40,41,44,46,47,50
+5VSS	4,28,31,32,35,39,40,41,42,43,44,46,47,48,51
+VCCSA	6,43
+VCCGT	7,43

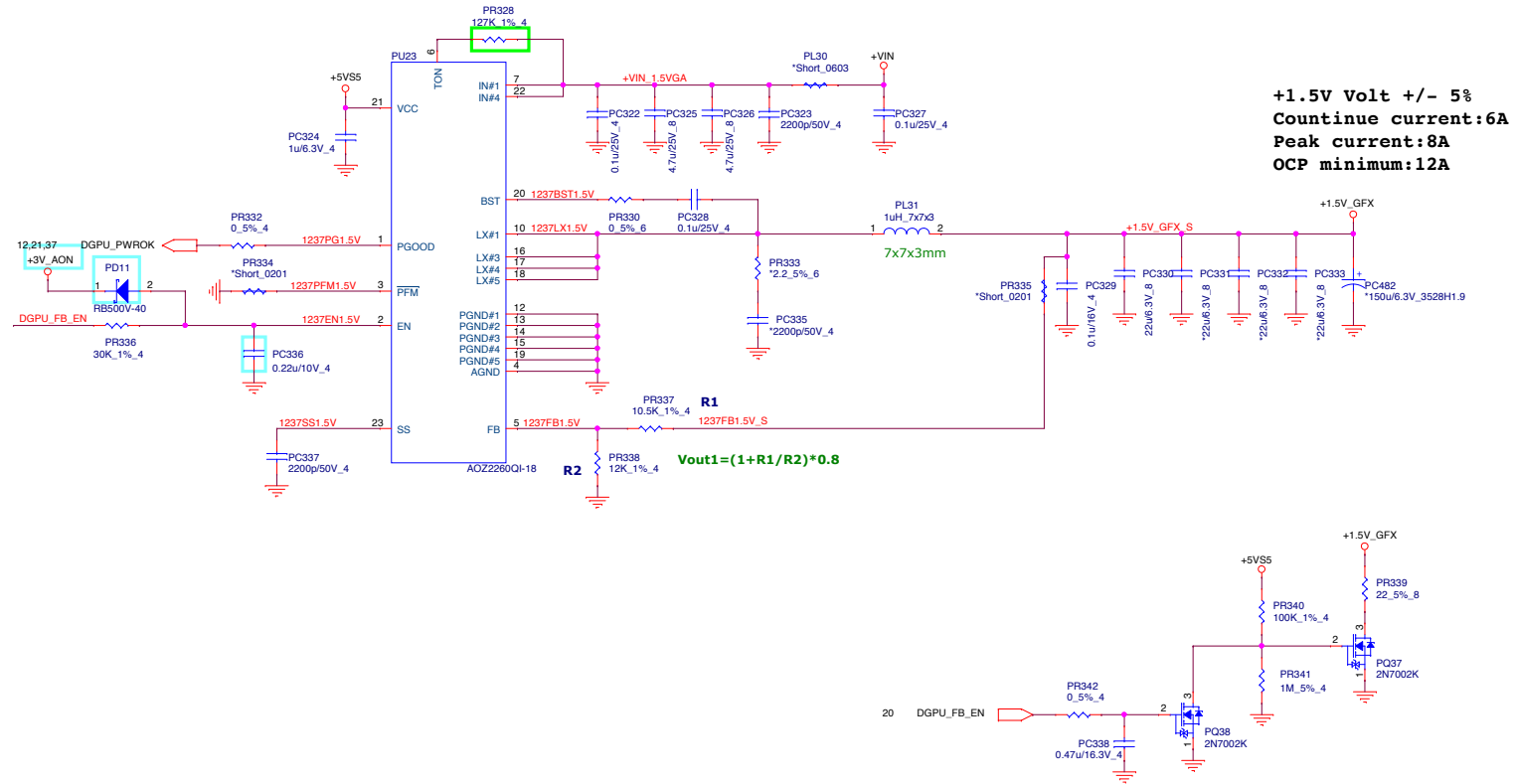




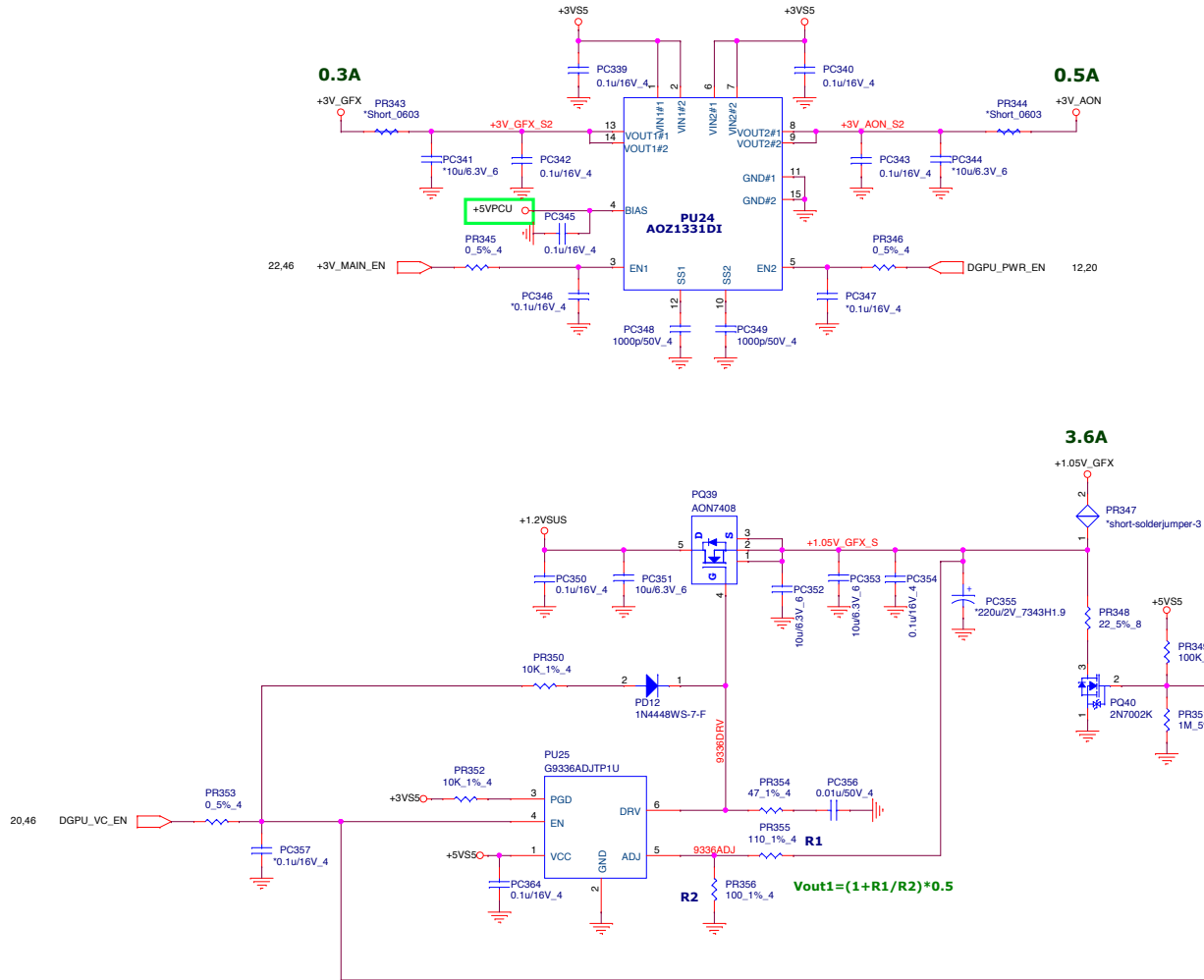
**N16S-GT (23/18W)**

EDP: 26A  
EDP peak: 51A  
OCP minimum 56A

+VIN 27,33,35,38,39,40,41,44,45,46,50  
 +5VS5 4,28,31,32,35,39,40,41,42,43,44,46,48,51  
 +1.5V\_GFX 20,21,23,24,25,26



+VIN	27,33,35,38,39,40,41,44,45,46,47,50
+3VS5	4,10,15,32,36,37,39,40,41,42,51
+5VS5	4,28,31,32,35,39,40,41,42,43,44,46,47,51
+3V_GFX	19,21,22,46
+3V_AON	19,22,47
+1.2VSUS	3,6,17,18,40,42
+1.05V_GFX	19,20,21

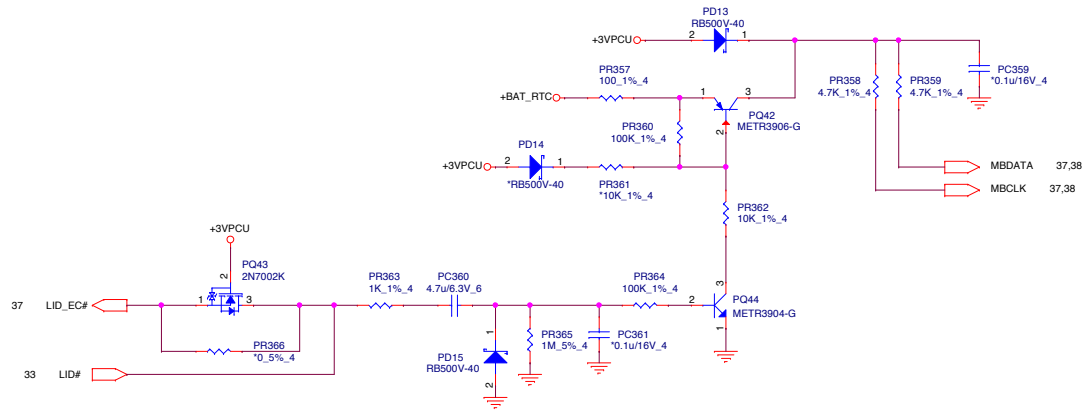


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**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>+3V/+1.05V_GFX(APL3523A)</b>	1A
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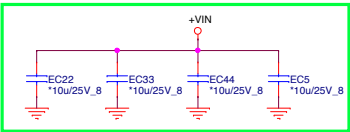
+3VPCU 6,13,31,32,33,36,37,38,39  
+BAT\_RTC 4,13,15,33,38



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